MOS/LSI DATABOOK

NATIONAL SEMICONDUCTOR

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SECTION 9
CONTROLLER ORIENTED PROCESSOR SYSTEMS (COPS)

COPS

National's Controller Oriented Processor Systems

introduction

National's Controller Oriented Processor Systems provide a low cost solution to low end computing and control problems. Manufactured by NSC's volume proven P-channel MOS/LSI controller process, the COPS offers an attractive, low risk alternative to custom LSI when available development time is short and cost is critical. Single mask programming of the on-chip control ROM allows delivery of prototype devices directly from the calculator production lines.

Architectural features of the COPS permit rapid efficient design and implementation of systems using key or switch inputs and display or printer outputs. Interface circuits in the COPS are designed to allow expansion of system memory and I/O capability without sacrificing the "lowest component count" features of the set.

Elements in the COPS family provide four levels of processing capability from the dedicated MM57140 single chip system with direct display and keyboard interface to the highly flexible MM5782 based multi-chip systems.

features

- National's COPS feature P-channel metal gate process for lowest cost
- Single power supply operation
- CMOS compatibility
- Serial I/O ports for easy communication between processor and peripheral circuits
- Expandable RAM and ROM
- BCD in/out option for applications flexibility
- Direct interfacing to keyboard and display
- 10 μs instruction cycle
- 4-bit data/8-bit instruction word
- Single mask programmable
- Learn mode programmability

COPS elements

- Automobile displays
- Oven controllers
- Vending machines
- Specialty calculators
- Simple electronic cash registers
- Computing instruments
- Electronic scales
- Printer/display controller
- Appliance controller
- Data terminal controller
- Automated gasoline pumps
- Alpha/numeric programmable calculators

applications

MM5781	– 16k control and ROM element
MM57129	– 32k control and ROM element
MM5782	– Memory and processor element
MM5785	– Memory interface to 1024 x 1 RAM devices
MM5788	– Printer interface to Seiko printers
MM5799	– Single chip microcomputer
MM57140	– Single chip microcomputer
DS8664/5/6	– Decoder, digit driver and oscillator
DS8692	– Hex power driver (single)
DS8693	– 8-bit latch and driver (source)
MM57126	– Programmer shift register

MM5781, MM5782 Controller Oriented Processor Systems

general description

The National MM5781, MM5782 is a set of MOS/LSI circuits designed for application in low cost, versatile, dedicated or custom programmed calculator and control systems.

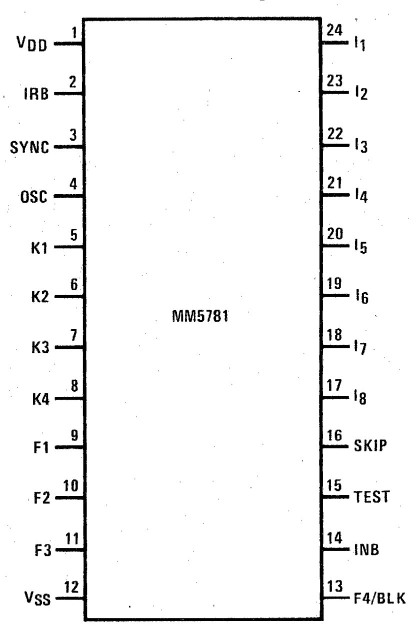
A full capability scientific or business calculator system can be built using only four circuits, plus the keyboard, case, battery and LED display. Application as a printing calculator or in electronic cash registers is possible using National's MM5788 printer interface circuit. Both the basic ROM instruction store and read/write store are expandable.

features

- 2048 x 8-bit ROM, expandable to 8192 x 8
- 640 bits (160 digits) RAM, expandable using MM5785
- 8 parallel outputs, coded as 7-segment + d.p. or BCD
- Serial data I/O for easy interface to peripheral circuits
- 3 general purpose I/O latches
- Blanking output
- 4 strobed key inputs
- 10μs micro-instruction cycle time
- Single power supply operation
- 4-bit data/8-bit instruction words

connection diagrams

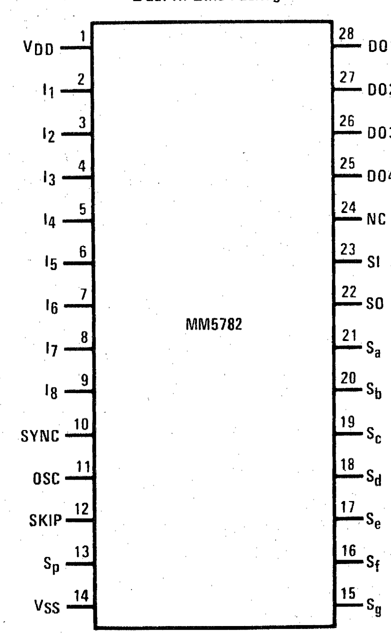
Dual-In-Line Package



TOP VIEW

Order Number MM5781N
See Package 22

Dual-In-Line Package



TOP VIEW

Order Number MM5782N
See Package 23

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All Other Pins Connected to V_{SS})	V_{SS} +0.3V to V_{SS} −12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

(0°C to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage ($V_{SS} - V_{DD}$)		7.9		9.5	V
Operating Supply Current (I_{DD})	$V_{SS} - V_{DD}$ = 9.5V, T_A = 25°C				
MM5781			−7	−12	mA
MM5782			−15	−25	mA
OSC Input Voltage Levels					
Logical High Level (V_{IH})	$V_{SS} - V_{DD}$ = 7.9V	V_{SS}−1.0			V
Logical Low Level (V_{IL})	$V_{SS} - V_{DD}$ = 9.5V			V_{DD}+1.5	V
OSC Input Resistance to V_{SS}	(Note 3), *(Figure 2)*				
MM5781 Only (R_{IN})			3	6	kΩ
INB, K1–K4, F1–F3 Input Voltage Levels					
Logical High Level (V_{IH})	$V_{SS} - V_{DD}$ = 7.9V	V_{SS}−3.2			V
	$V_{SS} - V_{DD}$ = 9.5V	V_{SS}−4.5			V
Logical Low Level (V_{IL})	7.9V ≤ $V_{SS} - V_{DD}$ ≤ 9.5V			V_{DD}+1.5	V
INB, K1–K4 Input Current Levels					
Logical High Level Current (I_{IH})	$V_{IH} = V_{SS}$ − 3.2V (LED Display Interface)			−350	µA
Logical Low Level Current (I_{IL})	$V_{IL} = V_{SS}$ − 32V (Fluorescent Display Interface)	−20		1	µA
IRB Input Voltage Levels					
Logical High Level (V_{IH})	7.9V ≤ $V_{SS} - V_{DD}$ ≤ 9.5V	V_{SS}−3.5			V
Logical Low Level (V_{IL})	$V_{SS} - V_{DD}$ = 7.9V			V_{DD}+2.5	V
	$V_{SS} - V_{DD}$ = 9.5V			V_{DD}+3.0	V
I_1–I_8, SI, SKIP, SYNC and TEST Input Voltage Levels	$V_{SS} - V_{DD}$ = 7.9V				
Logical High Level (V_{IH})		V_{SS}−1.2			V
Logical Low Level (V_{IL})				V_{SS}−4.0	V
DO 1, DO 2 and DO 4 Output Voltage Levels					
Logical High Level (V_{OH})	R_L = 150k, to V_{DD}	V_{SS}−1.0		V_{SS}	V
Logical Low Level (V_{OL})	I_{OL} = 3µA	V_{DD}		V_{DD}+0.5	V
Logical High Level Current (I_{OH})	$V_{OH} = V_{DD}$ + 1.5V, $V_{SS} - V_{DD}$ = 7.9V			−260	µA

dc electrical characteristics (con't)

(0°C to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DO 3 Output Voltage Levels					
Logical High Level (V_{OH})	R_L = 150k, to V_{DD}	$V_{SS}-1.0$		V_{SS}	V
Logical Low Level (V_{OL})	I_{OL} = 3µA	V_{DD}		$V_{DD}+0.5$	V
Logical High Level Current (I_{OH})	Battery Low "OFF"				
	$V_{OH} = V_{DD} + 3V$, $V_{SS} - V_{DD}$ = 9.5V	−1.3		−0.3	mA
	$V_{OH} = V_{DD} + 2.5V$, $V_{SS} - V_{DD}$ = 7.9V	−1.0		−0.4	mA
	Battery Low "ON"				
	$V_{OH} = V_{SS} - 3V$, $V_{SS} - V_{DD}$ = 7.9V			−0.3	mA
	$V_{OH} = V_{SS} - 3V$, $V_{SS} - V_{DD}$ = 9.5V			−0.4	mA
S_a through S_g and S_p Output Current Levels	LED Display Interface to DS8867				
Logical High Level Current (I_{OH})	$V_{OH} = V_{DD} + 5.4V$			−500	µA
Logical Low Level Current (I_{OL})	$V_{OL} = V_{DD} + 0.5V$	−1		1	µA
	Fluorescent Display Interface				
Logical High Level Current (I_{OH})	$V_{SS} - V_{DD}$ = 7.9V, $V_{OH} = V_{SS} - 6V$			−300	µA
Logical Low Level Current (I_{OL})	$V_{OL} = V_{SS} - 32V$, R_{EXT} = 150k to $V_{GG} = V_{SS} - 35V$	−20			µA
$I_1 - I_8$, S0, SYNC and SKIP Output Voltage Levels	$V_{SS} - V_{DD}$ = 7.9V				
Logical High Level (V_{OH})	I_{OH} = −100µA	$V_{SS}-0.5$		V_{SS}	V
Logical Low Level (V_{OL})	I_{OL} = 15µA	V_{DD}		$V_{DD}+3.7$	V
F1 – F3 Output Voltage Levels	$7.9V \leq V_{SS} - V_{DD} \leq 9.5V$				
Logical High Level (V_{OH})	I_{OH} = −30µA	$V_{SS}-1.5$			V
Logical Low Level (V_{OL})	I_{OL} = 3µA			$V_{DD}+1.0$	V
F4 (BLK) Output Voltage Levels	$7.9V \leq V_{SS} - V_{DD} \leq 9.5V$				
Logical High Level (V_{OH})	I_{OH} = −0.5 mA	$V_{SS}-1.5$			V
Logical Low Level (V_{OL})	I_{OL} = 5µA			$V_{DD}+1.0$	V
Voltage Levels for All Outputs into CMOS Level					
Logical High Level (V_{OH})	I_{OH} = −10µA	$V_{SS}-0.5$		V_{SS}	V
Logical Low Level (V_{OL})	R_L = 200k (to V_{DD})	V_{DD}		$V_{DD}+0.5$	V
Maximum Allowable Keyboard Closed Key Resistance Using INB, F1–F3 or K1–K4 as Inputs					
R_{KEY}	LED Display Interface			200	Ω
R_{KEY}	Fluorescent Display Interface			50	kΩ

ac electrical characteristics MM5781 – 0°C to +70°C, unless otherwise noted *(Figure 1)*

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSC Input Frequency ($1/t_p$)		320		400	kHz
OSC Input Duty Cycle		46	56	66	%
OSC Input Transition Times	(Note 3), *(Figure 2)*				
Fall Time (t_f)	C_L = 25 pF, R_L = 6 kΩ, to V_{SS}			50	ns
Rise Time (t_r)	RC = 0.15µs			350	ns
SYNC Input Timing (Bit Time)					
Interval Time (t_b)		10		12.5	µs
Hold Time (t_{osch})		100			ns
High-to-Low Set-Up Time (t_{stl})		680			ns
Low-to-High Set-Up Time (t_{sth})		100			ns
K1 – K4, INB, F1 – F3 Input Timing					
Set-Up Time (t_{sk})		6.5			µs
Hold Time (t_{hk})		1.0			µs
SKIP Input Timing					
Set-Up Time (t_{sx})		280			ns
Hold Time (t_{hx})		1.0			µs
IRB, $I_1 - I_8$ Input Timing					
Set-Up Time (t_{si})		1.75			µs
Hold Time (t_{hi})		1.0			µs
SKIP Output Propagation Delay (t_{pdx})	C_{LOAD} = 250 pF			4.4	µs
$I_1 - I_8$ Output Propagation Delays	C_{LOAD} = 250 pF				
Low-to-High (t_{pdhi})				3.6	µs
High-to-Low (t_{pdli})				3.0	µs
F1 – F3 Output Propagation Delay (t_{pdf})	C_{LOAD} = 100 pF			4.4	µs
F4 Output Propagation Delay (t_{pdf})	C_{LOAD} = 50 pF			4.4	µs
F4 Output Transition Time					
Rise Time (t_r)	$C_{LOAD} \geq$ 20 pF	0.3			µs

timing diagram (See notes in *Figure 2.*)

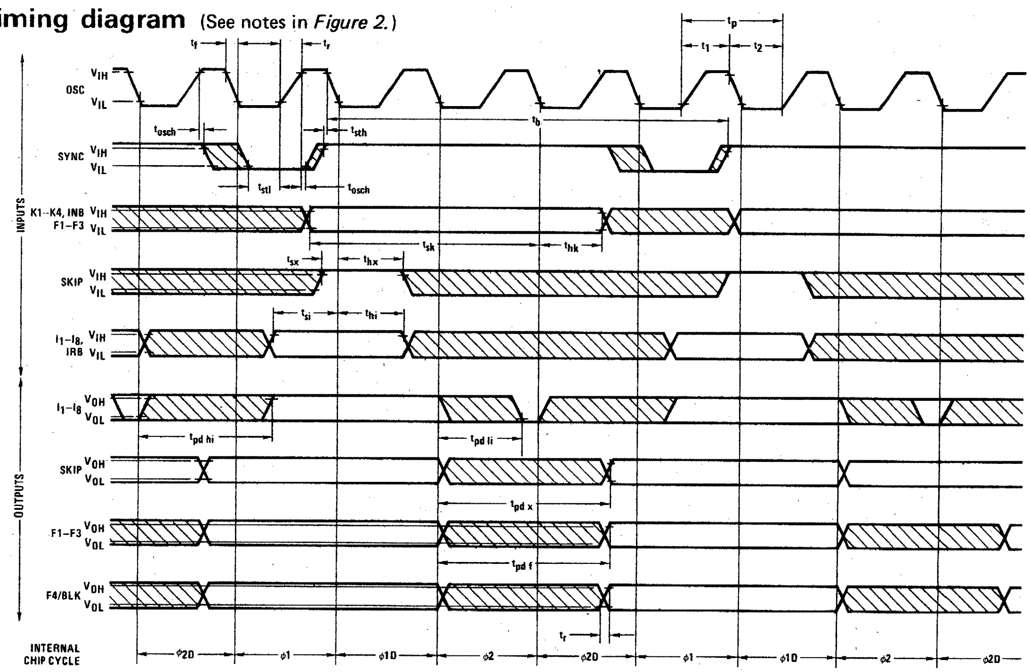
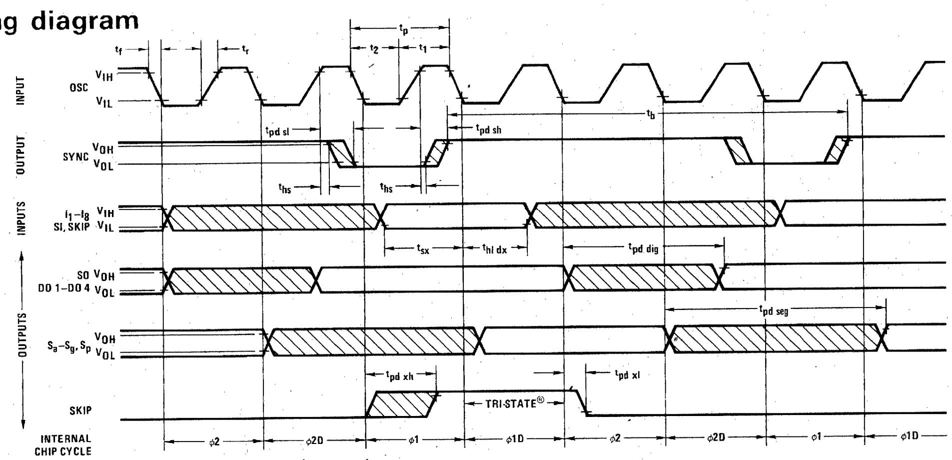


FIGURE 1. MM5781 Input/Output Waveform Timing

ac electrical characteristics MM5782 – 0°C to +70°C, unless otherwise noted *(Figure 2)*

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSC Input Frequency ($1/t_p$)		320		400	kHz
OSC Duty Cycle		46	56	66	%
OSC Input Transition Times					
Rise Time (t_r)	RC = 0.15µs			350	ns
Fall Time (t_f)	C_L = 25 pF, R_L = 6 kΩ to V_{SS}			50	ns
SYNC Output Cycle (t_b, Bit Time)	320 kHz ≤ f_{OSC} ≤ 400 kHz	10		12.5	µs
SYNC Output Timing	C_L = 250 pF				
High-to-Low Propagation Delay (t_{pdsl})		0.1		1.65	µs
Low-to-High Propagation Delay (t_{pdsh})		0.1		1.25	µs
Initial Transition Delay (t_{hs})		0.1		0.8	µs
$I_1 - I_8$, SI and SKIP Input Timing					
Set-Up Time (t_{sx})		1.5			µs
Hold Time (t_{hldx})		0.5			µs
DO 1 – DO 4 and S0 Propagation Delay (t_{pddig})	C_L = 100 pF (DO 1 – DO 4) C_L = 250 pF (S0 Only)	0.5		4	µs
$S_a - S_g$, S_{dp} Propagation Delay (t_{pdseg})	C_L = 100 pF			6.0	µs
SKIP Output Timing	C_L = 250 pF				
t_{pdxh}				2.4	µs
t_{pdxl}				2.4	µs
t_{hx}		0.1			µs
Interdigit Blanking Time	*(Figure 5)*				
T1	t_b = 10µs,	6.5	7.5		µs
Display Blanking	*(Figure 5)*				
T1 + T2 + T4	t_b = 10µs,	38	40		µs

timing diagram



Note 1: OSC input duty cycle = $\frac{t_1}{t_1 + t_2} = \frac{t_1}{t_p}$

Note 2: SYNC provides a 1 of 4 timing relationship with OSC input, to establish OSC edges as references for the I/O timing.

Note 3: OSC output rise time is determined by capacitive loading and programmable pull-up resistor at the MM5781 input, programmed to provide R_C ≤ 0.15µs.

FIGURE 2. MM5782 Input/Output Waveform Timing

functional description

MM5781 CONTROL ROM ELEMENT (CRE)

Sixteen kilobits of ROM are organized as 32 pages of 64 8-bit instruction words each. Eight instruction lines and a SKIP signal interconnect the ROM with the MM5782 MPE circuit. Addressing is by an 11-bit P.C. register with two 11-bit push-down address save registers. Four dynamic switch inputs K1–K4 and a static switch input (INB) allow scanning of up to 56 keys and 14 static switches directly. A sixth input (IRB) drives an internal latch that can be used as a program controlled interrupt function.

There are also three program definable I/O ports (F1 – F3) and an additional blanking output F4. The F1–F4 outputs are latched. Four MM5781's may be used with a single MM5782 without additional interface circuits. *Figure 3* shows the MM5781 logic diagram.

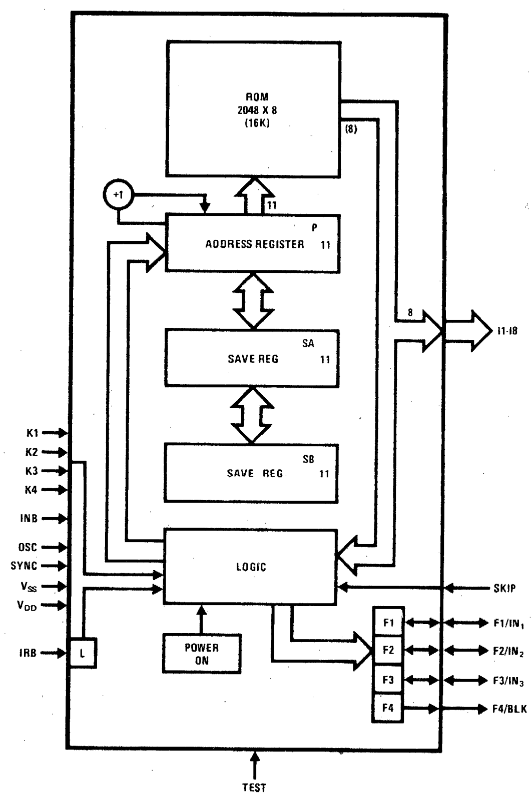


FIGURE 3. MM5781 Control and ROM Element

MM5782 MEMORY AND PROCESSOR ELEMENT (MPE)

The MPE contains 640 bits of RAM organized as 10 16-digit registers. Other register lengths are possible under control of the program. The RAM is addressed by the 8-bit B register. The upper 4 bits (B_r) select a particular register and the lower 4 bits (B_d) address the 4-bit words with the register.

Arithmetic and logic functions are performed by the 4-bit binary adder with results stored in the accumulator. The C flip-flop is used for carry bit storage, display decimal point location, and may be utilized to control the skip instruction.

Digit timing information for external keyboard scanning and for driving displays is encoded into a 4-bit code and presented on the DO1–DO4 lines. Eight outputs are decoded by the segment PLA and brought out as 7 segments, BCD, or individually set outputs under program control. Display output timing is shown in *Figure 5*.

Serial data may be transferred from and into the accumulator A on the Serial Input (SI) and Serial Output (SO) lines. Decimal point position for serial data is given on S_p.

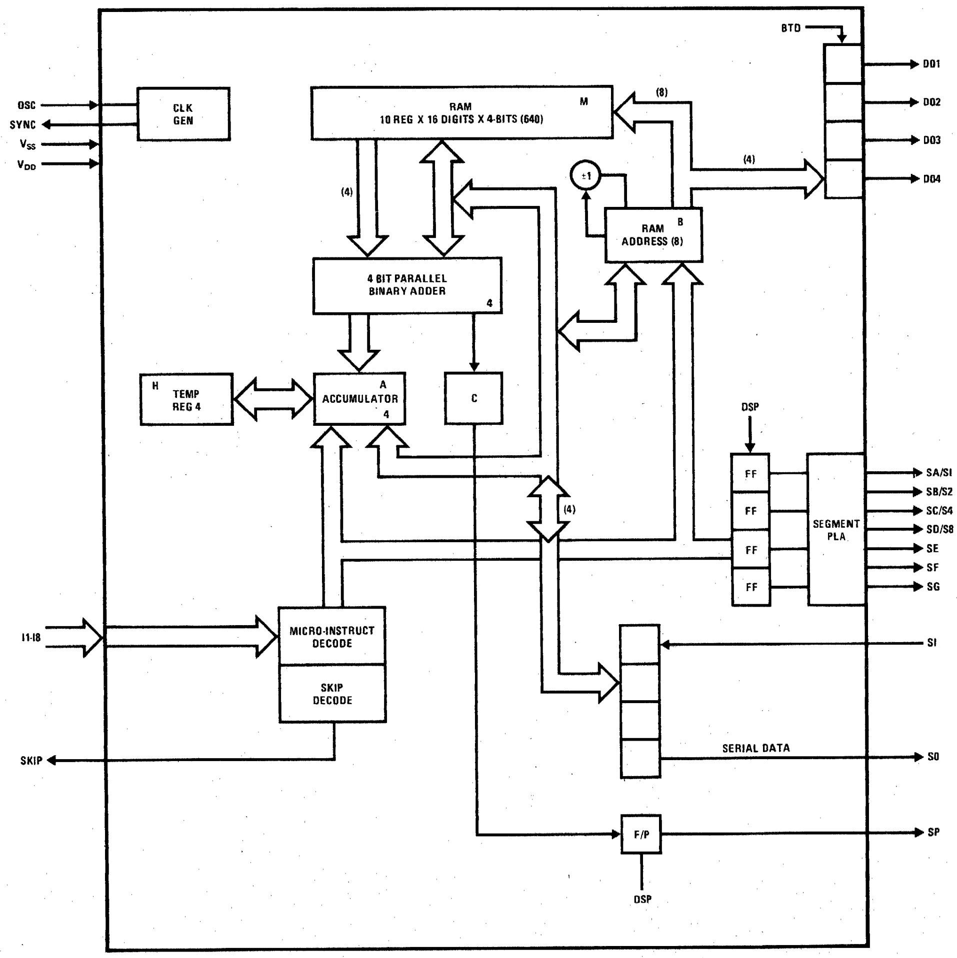
The MM5782 logic diagram is shown in *Figure 4*. Tables I and II list the instruction set and corresponding ROM Codes for the MM5781, MM5782 System.

TYPICAL CALCULATION TIMES

System calculation times will vary with the programmed algorithms. The formulas listed reflect one method.

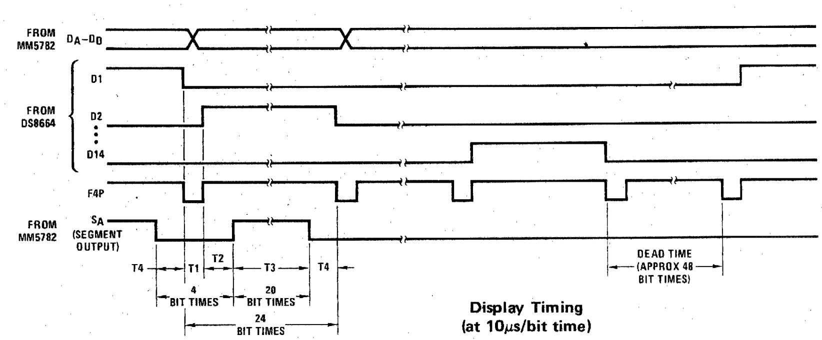
- Time to add or subtract two numbers:
  $T = ((2N + 20)\ M + 5N + 10)\ t_b$
  where
  N = number of digits per register
  t_b = bit time = 10μs nominal
  M = number of shifts required to align decimal point
- Time to multiply two N-Digit numbers:
  $T = ((5N + 15)\ P + (4N + 20)\ N + 10)\ t_b$
  where
  P = sum of multiplier digits, i.e., if multiplier = 3211, P = 3 + 2 + 1 + 1 + = 7
- Time to divide two N-digit numbers:
  $T = ((5N + 15)\ S + (14N + 40)\ N + 10)\ t_b$
  where
  S = sum of digits in answer, i.e., if answer = 1234, S = 1 + 2 + 3 + 4 = 10
- Time to enter a BCD number:
  $T = 13N\ t_b$

functional description (con't)



28 PIN

FIGURE 4. MM5782 Memory and Processor Element



Display Timing
(at 10μs/bit time)

T1 = 7.5μs = Digit Blanking
T2 = 17.5μs
T3 = 200.0μs
T4 = 15.0μs

Digit time = 240.0μs with 7.5μs digit blanking and 40μs segment blanking

Note 1: Duty cycle = $\frac{200}{240 \times 16} = \frac{1}{19.2} = 5.2\%$

FIGURE 5. Display Output Timing

typical applications

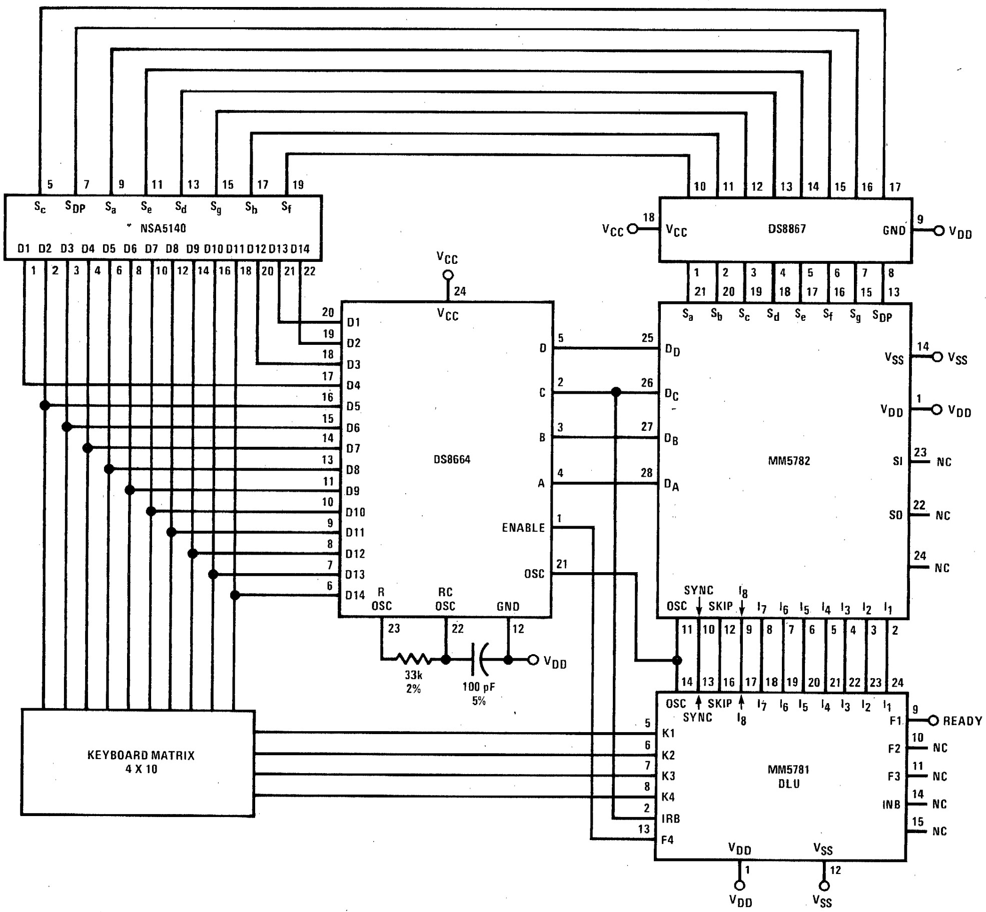


FIGURE 6. Typical 10-Digit Scientific Calculator

Typical application of the MM5781, MM5782 set as a scientific calculator is shown in *Figure 6*. The MM5781 may be programmed to interface with most low cost keyboards which are often the least desirable from a false or multiple entry viewpoint.

When a key closure is sensed by the MM5781, an internal timeout may be programmed to occur. Noise voltages of significant magnitude which occur on the K1–K4 inputs cause the timeout period to be restarted. In this way a key closure is accepted as valid only after a predetermined noise-free period of time. Key release may be validated in the same manner.

typical applications (con't)

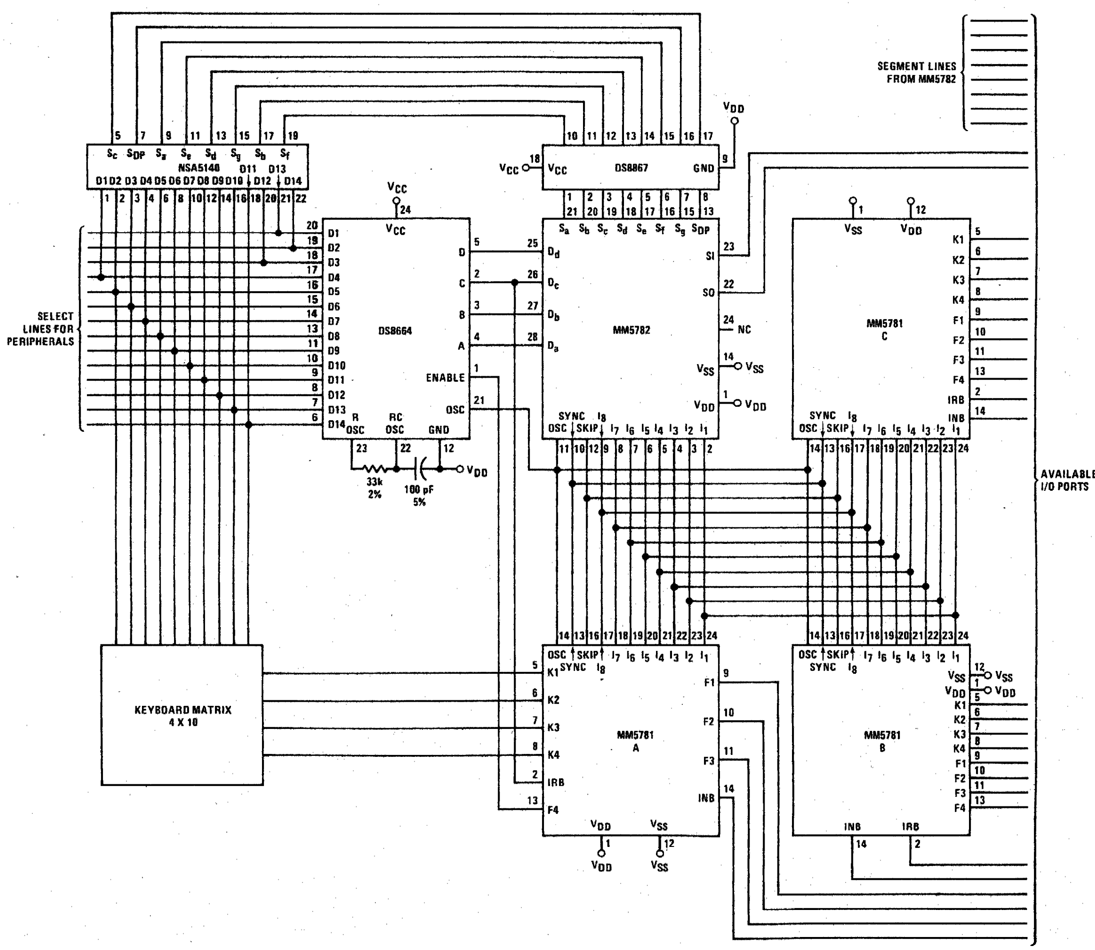


FIGURE 7. Multi-ROM System (Controller, Etc.)

Versatility of the COP set is illustrated in *Figure 7*, showing a multiple ROM system configured for an industrial controller application.

In this application, Control ROM A is programmed to debounce the keyboard inputs as described above. Control ROMs B and C utilize the K1–K4 lines as general purpose wired inputs. If additional RAM is required, the MM5785 RAM Interface chip allows up to four 1024 x 1 RAMs to be accessed through the SI and SO parts of the MM5782.

register and I/O port definitions

TABLE I.

DESCRIPTIONS	DESIGNATIONS
MPE – MEMORY AND PROCESSOR ELEMENT	
640-Bit RAM 10 Registers x 16 Digits x 4 Bits (r x d x z)	M
8-Bit RAM Address Register	B
B_r (Register) B_d (Digit)	
4-Bit Accumulator	A
4-Bit Holding Register	H
1-Bit Carry Register	C
1 Latched Output (Decimal Point)	S_p
4 Latched Digit Outputs	DO4–DO1
4 Latched Segment Outputs: Direct or Decoded to 7-Segment Outputs	S_a–S_g
Serial Input and Output	SI–SO
CRE – CONTROL AND ROM ELEMENT	
16,384-Bit ROM	I_8–I_1
11-Bit Program Address Register	P
Page P_p (P11 – P7) Word P_w (P6 – P1)	
2 x 11-Bit Program Address Save Registers	S_{A1}–S_{A11} S_{B1}–S_{B11}
4 General Purpose Flags (Latched)	F1–F4
4 Keyboard Inputs	K1–K4
Static Switch Input	INB
Interrupt Input	IRB

standard instructions

	MNEMONIC	DATA FLOW	STATUS – SKIP IF	DESCRIPTION
Memory Digit Operations	EXC (r)	A ↔ M (B) $B_r \oplus r \rightarrow B_r$		Exchange data word at M(B) with A EXCLUSIVE-OR B_r with r. r = 0, 1, 2, 3
	EXC –(r)	A ↔ M (B) $B_r \oplus r \rightarrow B_r$, $B_d - 1 \rightarrow B_d$	$B_d \rightarrow 15$	Exchange and decrement B_d EXCLUSIVE-OR B_r with r
	EXC +(r)	A ↔ M (B) $B_r \oplus r \rightarrow B_r$, $B_d + 1 \rightarrow B_d$	$B_d \rightarrow 0$ or $B_d \rightarrow 13$	Exchange and increment B_d EXCLUSIVE-OR B_r with r
	MTA (r)	M (B) → A $B_r \oplus r \rightarrow B_r$		Load accumulator with data word at M (B) EXCLUSIVE-OR B_r with r
	LM (Y)	Y → M (B) $B_d + 1 \rightarrow B_d$		Load memory with Y, Y = 0, 1, 2,. . . 15 Increment B_d
Memory Bit Operations	SM (Z)	1 → M (B, Z)		Set bit Z of M (B), Z = 1, 2, 4, 8
	RSM (Z)	0 → M (B, Z)		Reset bit Z of M (B)
	TM (Z)		M (B, Z) = 0	Test bit Z of M (B), skip if zero
Memory Address Operations	LB (r, d)	$r \rightarrow B_r$, $d \rightarrow B_d$		r = 0, 1, 2, 3. d = 0, 11, 12, 13, 14, 15 Load B register. Successive LB's are ignored
	LBL (I)	$I_{8-5} \rightarrow B_r$, $I_{4-1} \rightarrow B_d$		2 microcycle instruction. Load next ROM word into B register
	ATB	$A \rightarrow B_d$		Transfer contents of accumulator to B_d register
	BTA	$B_d \rightarrow A$		Transfer contents of B_d register to accumulator
	HXBR	H ↔ B_r		Exchange contents of H and B_r registers

standard instructions (con't)

	MNEMONIC	DATA FLOW	STATUS – SKIP IF	DESCRIPTION
Control Functions	GO TO (GO)	$I_6 - I_1 \rightarrow P_W$ If P_P = 1111X:11110 $\rightarrow P_P$		Load next ROM instruction address. If on page 36_8 or 37_8 reset page address to 36_8
	CALL	$I_6 - I_1 \rightarrow P_W$, IIIII $\rightarrow P_P$ If $P_P \neq$ IIIIX: $S_A \rightarrow S_B$, $P + 1 \rightarrow S_A$		Call subroutine. If not page 36_8 or 37_8, set page address to 37_8. Push down address save registers
	RET	$S_A \rightarrow P$ $S_B \rightarrow S_A$, $S_B \rightarrow S_B$		Pop up ROM address save registers
	RETS	$S_A \rightarrow P$ $S_B \rightarrow S_A$, $S_B \rightarrow S_B$	SKIP	RET, then skip next instruction upon return
	LG/GO	Load P		2 microcycle operation, long GO TO, load P_P and P_W
	LG/CALL	$S_A \rightarrow S_B$, $P + 1 \rightarrow S_A$ Load P		2 microcycle operation. Long call. Load P_P and P_W. Push down address save registers
	CALX (N)	In active CRE – $P + 1 \rightarrow S_A$ $S_A \rightarrow S_B$ $0 \rightarrow P$ In selected CRE – $I_6 \rightarrow I_1 \rightarrow P_W$ $0 \rightarrow P_P$		2 microcycle operation, N = 1, 2, 3. Call additional CRE (N). Push down address save registers of active CRE. Load P of selected CRE (N) from next instruction word
	RTX (0)	In active CRE – $P + 1 \rightarrow S_A$, $S_A \rightarrow S_B$ $0 \rightarrow P$ In CRE (O) – $S_A \rightarrow P$ $S_B \rightarrow S_A$		2 microcycle operation. Return to CRE (O). Pop up ROM address save registers in CRE (O). Push down ROM address save registers of active CRE
	NOP			No operation
Arithmetic Operations	AD	$M + A \rightarrow A$		Add M (B) to A, store sum in A
	ADD	$C + M + A \rightarrow A$ $0 \rightarrow C$ if $A < 10$ $1 \rightarrow C$ if $A \geq 10$	$A < 10$	Add carry bit to M (B), add sum to A, store sum in A Set C if $A \geq 10$, reset C if $A < 10$
	SUB	$M + \bar{A} + C \rightarrow A$ Overflow $\rightarrow$ C	Overflow	Subtract A from M Overflow to C
	COMP	$\bar{A} \rightarrow A$		One's complement of A to A
	0TA	$0 \rightarrow A$		Clear accumulator
	ADX (Y)	$A + Y \rightarrow A$	No overflow, $Y \neq 6$	Add constant (Y) to A, store sum in A Y = 1, 2, . . . 15
	HXA	$H \leftrightarrow A$		Exchange contents of H register with A
	TAM		A = M (B)	Compare contents of A to M (B), skip if A = M (B)
	SC	$1 \rightarrow C$		Set C register
	RSC	$0 \rightarrow C$		Reset C register
	TC		C = 0	Skip if C = 0
Input/Output	BTD	$B_d \rightarrow$ DO4 – DO1		Transfer contents of B_d to digit output latches
	DSPA	$A \rightarrow S_a - S_d$ $0 \rightarrow S_e - S_g$ $C \rightarrow S_p$		A4–A1 to output latches, directly to outputs S_a–S_d 0 to outputs S_e–S_g C to S_p latch
	DSPS	$A \rightarrow S_a - S_g$ $C \rightarrow S_p$		A to output latches, 7-segment decoded to S_a–S_g C to S_p latch
	AXO	$SI \rightarrow A$ $A \rightarrow SO$		Exchange accumulator with serial input/output
	LDF	$I \rightarrow F$ (N)		N = 1, 2, 3, 4. Load F (N) from next instruction word 2 microcycle instruction
Input Test	TIN		INB = 1	Test INB. Active state of input is programmable
	TK (N)	if F4 = 0 if F4 = 1	K (N) = 1 F (N) = 1	N = 1, 2, 3, 4. Active state of input is programmable N = 1, 2, 3
	TKB		K (N) = 1	N = 1, 2, 3, 4. Skip if any K input active
	TIR		ΔIRB	Test IRB. Skip if IRB has changed since last test of IRB

operation codes

TABLE II.

OP CODE				MNEMONIC			
I_8 I_7	I_6 I_5	I_4 I_3	I_2 I_1	00	01	10	11
00	XX	00	00	NOP	DSPA	COMP	OTA
00	XX	00	01	HXB$_r$	DSPS	AXO	HXA
00	XX	00	10	ADD	AD	SUB	TAM
00	XX	00	11	SC	LBL	RSC	LDF
00	XX	01	00	TK1	TK2	TK3	TK4
00	XX	01	01	TIR	TKB	BTD	TIN
00	XX	01	10	MTA (r)			
00	XX	01	11	EXC (r)			
00	XX	10	00	EXC– (r)			
00	XX	10	01	EXC+ (r)			
00	XX	10	10	LB (r, 0)			
00	XX	10	11	LB (r, 11)			
00	XX	11	00	LB (r, 12)			
00	XX	11	01	LB (r, 13)			
00	XX	11	10	LB (r, 14)			
00	XX	11	11	LB (r, 15)			
01	00	00	XX	RET	RETS	RSM (8)	BTA
01	00	01	XX	TM (1)	TM (2)	TM (4)	TM (8)
01	00	10	XX	RSM (1)	SM (1)	SM (8)	RSM (4)
01	00	11	XX	RSM (2)	TC	SM (2)	SM (4)
01	01	00	XX	ATB	ADX (1)	ADX (2)	ADX (3)
01	01	01	XX	ADX (4)	ADX (5)	ADX (6)	ADX (7)
01	01	10	XX	ADX (8)	ADX (9)	ADX (10)	ADX (11)
01	01	11	XX	ADX (12)	ADX (13)	ADX (14)	ADX (15)
01	10	00	XX	CALX	LG (35, 34)	LG (33, 32)	LG (31, 30)
01	10	01	XX	LG (27, 26)	LG (25, 24)	LG (23, 22)	LG (21, 20)
01	10	10	XX	LG (17, 16)	LG (15, 14)	LG (13, 12)	LG (11, 10)
01	10	11	XX	LG (7, 6)	LG (5, 4)	LG (3, 2)	LG (1, 0)
01	11	00	XX	LM (0)	LM (1)	LM (2)	LM (3)
01	11	01	XX	LM (4)	LM (5)	LM (6)	LM (7)
01	11	10	XX	LM (8)	LM (9)	LM (10)	LM (11)
01	11	11	XX	LM (12)	LM (13)	LM (14)	LM (15)
10	XX	XX	XX	CALL			
11	XX	XX	XX	GO			

MM5785 RAM interface chip

general description

The MM5785 provides the required level conversion between the MM5782 or MM5799 Controller Oriented Processors and external RAM memory. It is intended for use with the MM74C930 and MM2102 1k RAMs as a means of expanding system data storage capability.

The MM5785 RAM Interface Element allows direct connection of four 1024 x 1 organized read/write memories to the processor. *Figure 1* is a block diagram of the element. Additional interface elements may be added using decoded digit lines from the decoder/driver as chip selects.

The chip contains a 9-stage address and control bit holding register, a 6-bit incrementing register, control logic and data buffers. A power-on sequence resets all registers when power is applied. *(Figure 5.)*

In operation, the chip select is energized and a synchronizing bit followed by the R/W mode select bit, four chip select bits (CSA–CSD), and the register select address bits (A9–A6) are shifted into the holding register (R) through the D_{IN} input port. The 6-bit address register then sequentially addresses each of the 64 bits within the selected register. In the Write mode, data to be stored is transferred from the processor on the D_{IN} line and outputted to the memory on the DOR line. When reading, data flow is from the memory chip to the DIR pin. The data is buffered and shifted out to the processor on the DO line. All registers are cleared when the address sequence is complete.

Four to sixteen line decoding of the CSA–CSD lines allows addressing of as many as sixteen 1024-bit RAMs using a single MM5785. When interfacing memory circuits such as the MM74C930 or MM2102 to the MM5785, one transistor is required for the CSR (BAM control) line as shown in *Figure 2*.

features

- Directly interfaces the MM5782 and MM5799 Controller Oriented Processors to external RAM
- Compatible with low power CMOS MM74C130 or low cost MM2102 RAM
- Internal power-on clear

block and connection diagrams

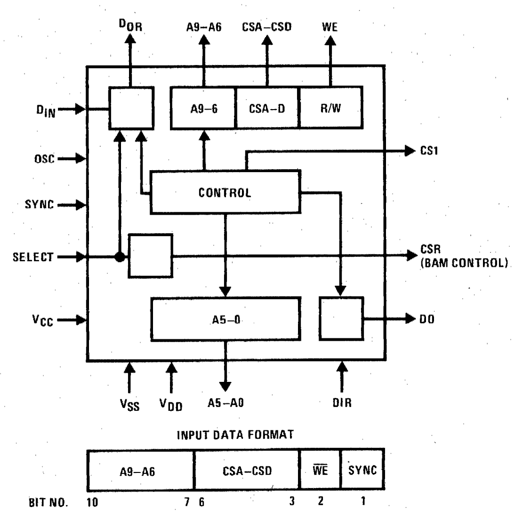
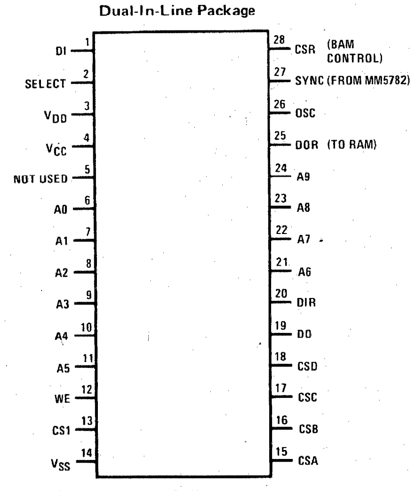


FIGURE 1. MM5785 RAM Interface Element

Dual-In-Line Package



Order Number MM5785N
See Package 23

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All Other Pins Connected to V_{SS})	V_{SS} + 0.3V to V_{SS} − 12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$7.9V \leq V_{SS} - V_{DD} \leq 9.5V$, $4.5V \leq V_{CC} - V_{DD} \leq 5.5V$
(V_{SS} is always the most positive supply voltage)

dc electrical characteristics (T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Operating Supply Current	$V_{DD} = V_{SS} - 9.5V$		8	15	mA
I_{CC}	Operating Supply Current	Capacitive Loading Only			100	μA
I_{CC}	Peak Current	C_L = Max, R_L = Open Circuit, Duration = 400 ns			33	mA
	OSC Input Levels					
V_{IH}	Logical High Level	$V_{DD} = V_{SS} - 7.9V$	V_{SS}−1.0			V
V_{IL}	Logical Low Level	$V_{DD} = V_{SS} - 9.5V$			V_{DD}+1.5	V
	D_{IN}, SYNC Input Levels					
V_{IH}	Logical High Level	$V_{DD} = V_{SS} - 7.9V$	V_{SS}−1.2			V
V_{IL}	Logical Low Level	$V_{DD} = V_{SS} - 9.5V$			V_{SS}−4.0	V
	DIR Input Levels					
V_{IH}	Logical High Level		V_{DD}+2.0			V
V_{IL}	Logical Low Level				V_{DD}+0.4	V
	Select Input Levels					
V_{IH}	Logical High Level	$V_{DD} = V_{SS} - 7.9V$	V_{SS}−3.2			V
V_{IL}	Logical Low Level	$V_{DD} = V_{SS} - 9.5V$	V_{SS}−4.5		V_{DD}+1.5	V
					V_{DD}+1.5	V
I_{IH}	Input Current Level	$V_{IH} = V_{SS} - 3.2V$, $V_{DD} = V_{SS} - 7.9V$	−350			μA
	CSR Output Levels					
V_{OH}	Logical High Level	$I_{OH} \leq -100$ μA	V_{DD}+0.8			V
V_{OL}	Logical Low Level	$I_{OL} \leq 10$ μA			V_{DD}+0.25	V
	DOR, WE, CS 1, A0–A9 and CSA–CSD Output Levels					
V_{OH}	Logical High Level	$I_{OH} \leq -250$ μA	V_{CC}−1.0			V
V_{OL}	Logical Low Level	$I_{OL} \geq 10$ μA			V_{DD}+0.5	V
	DO Output Levels					
V_{OH}	Logical High Level	$V_{DD} = V_{SS} - 7.9V$, $I_{OH} \leq -100$ μA	V_{SS}−0.5			V
V_{OL}	Logical Low Level	$V_{DD} = V_{SS} - 7.9V$, $I_{OL} \geq 25$ μA			V_{DD}+3.7	V

ac electrical characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	OSC Input Frequency ($1/t_p$)		320		400	kHz
	OSC Duty Cycle	*(Figure 3)*	46	56	66	%
	OSC Input Transition Times					
t_r	Rise Time	RC = 0.15 µs			350	ns
t_f	Fall Time	C_L = 25 pF, R_L = 6 kΩ			50	ns
	SYNC Input Timing	*(Figure 3)*				
t_B	Interval/Bit Time		10.0		12.5	µs
t_{osch}	Hold Time		100			ns
t_{stL}	High-to-Low Set-Up Time		680			ns
t_{stH}	Low-to-High Set-Up Time		100			ns
	DIN Input Timing					
t_{stn}	Set-Up Time		2.5			µs
t_{hn}	Hold Time		1.0			µs
	DIR Input Timing	$C_L \leq 50$ pF				
t_{str}	Set-Up Time		2.5			µs
t_{hr}	Hold Time		1.0			µs
	SELECT Input Timing The SELECT Input is normally 75 bits wide and envelopes the DIN input. The DOR output is the logical-OR of $\overline{\text{SELECT}}$ and DIN	$C_{LOAD} \leq 100$ pF, *(Figure 4)*				
	DOR, A0–A9 Output Propagation Delays	C_{LOAD} = 250 pF				
t_{pdL}, t_{pdH}					5.0	µs
	CSA–CSD Output Propagation Delays	C_{LOAD} = 100 pF				
t_{pdL}					5.0	µs
t_{pdH}					10.0	µs
	WE and CS 1 Output Propagation Delays	C_{LOAD} = 250 pF				
t_{pdL}, t_{pdH}					2.5	µs
	DO Output Propagation Delays	C_{LOAD} = 100 pF				
t_{pdL}, t_{pdH}					2.5	µs
	V_{SS} Power "ON" Time					
t_{po}		*(Figure 5)*			1.0	ms

functional description

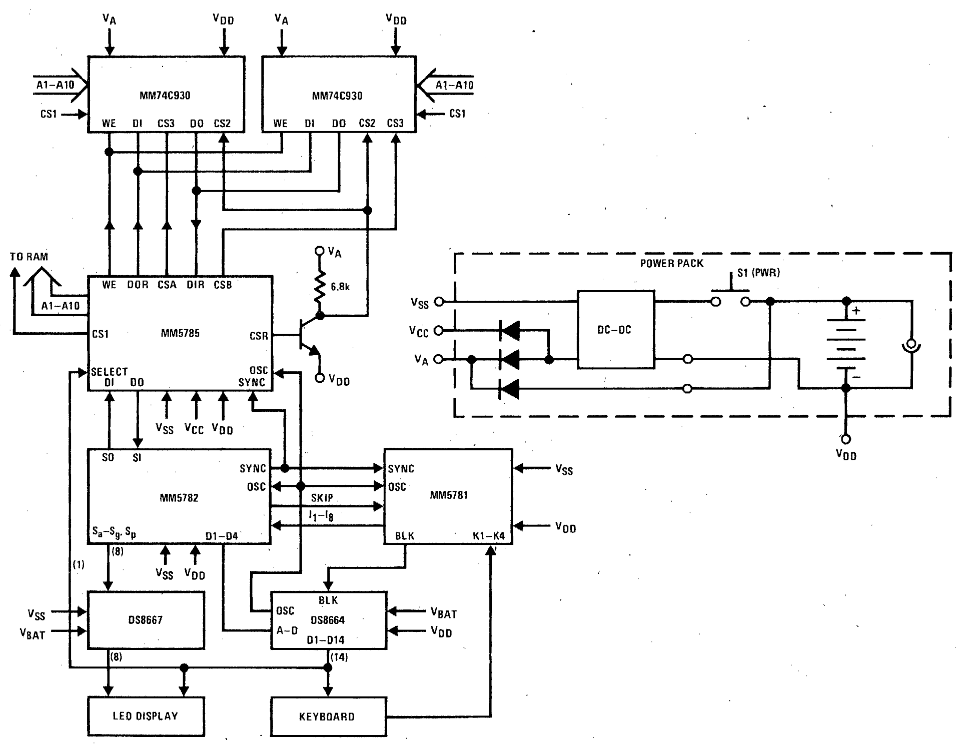


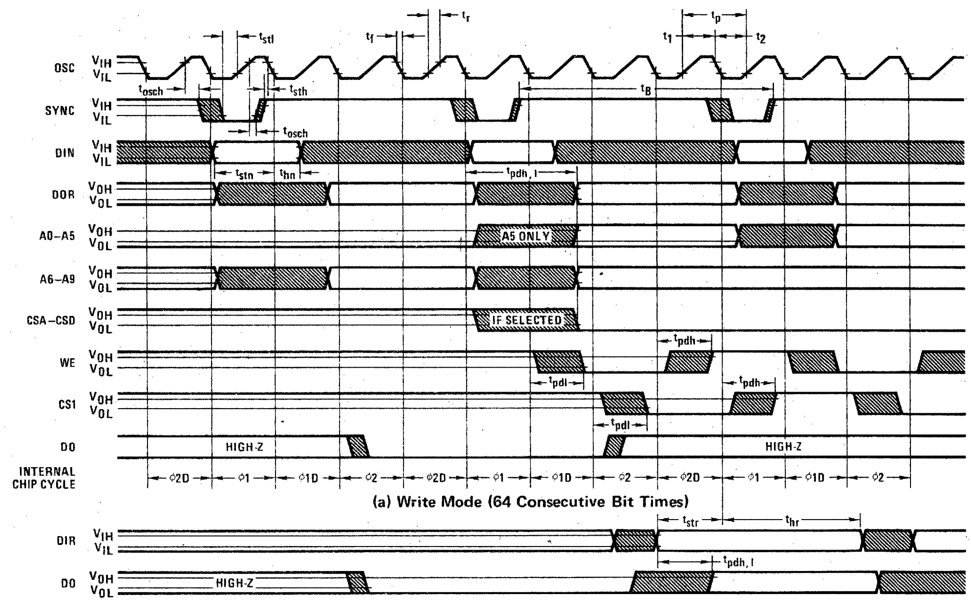
FIGURE 2. Hand-Held Calculator with Battery Augmented Memory (BAM)

A power-on sequence is necessary to clear all registers and condition the MM5785 for data entry. Timing is described in *Figure 5*. Select must be toggled once before starting.

An interface circuit is required in a non-volatile battery back-up system using the MM74C930. An example is shown in *Figure 6*. Before the MM5785 is selected, P_{ON} is at a logical high level, Q1 is "OFF," and the RAMs are disabled. If system power is removed, V_{SS} collapses to Gnd, Q1 remains "OFF" so that false data cannot be entered during power up.

During normal operation, P_{ON} is in a logical low state and when the MM5785 is selected, Q1 turns "ON" to enable the RAMs. R_L is chosen from the CSR I_{OH} spec to insure saturation of Q1. CSR timing is shown in *Figure 5*.

functional description (Continued)



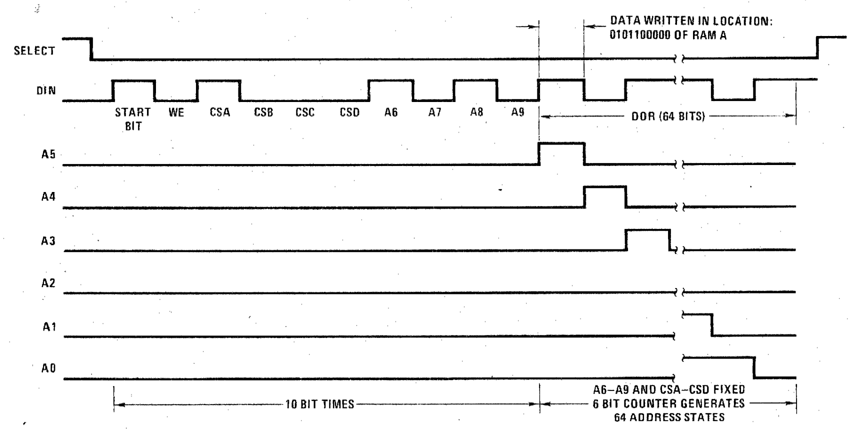
(a) Write Mode (64 Consecutive Bit Times)

(b) Read Mode (WE at Logical High Level. A0–A9, CSA–CSD and CS1 have Same Timing as Write Mode)

Note 1. Osc input duty cycle = $\frac{t_1}{t_1 + t_2} = \frac{t_1}{t_p}$

Note 2. SYNC provides a 1 of 4 timing relationship with osc input, to establish osc edges as references for I/O timing.

FIGURE 3. Input/Output Waveform Timing



Start bit is always positive logic "1," logical high level

The above pattern indicates a write condition with CSA selected.

FIGURE 4. Typical Bit Pattern

functional description (Continued)

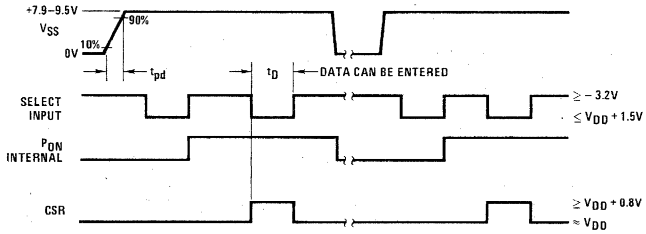


FIGURE 5. Power-Up Timing

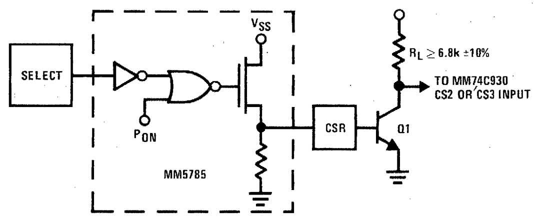


FIGURE 6

MM5788 printer interface chip

general description

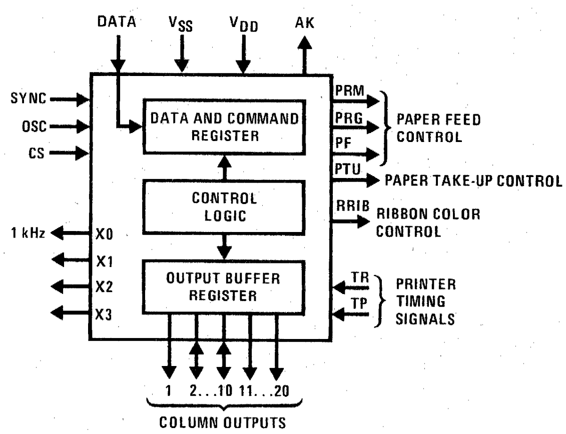
The MM5788 is an MOS/LSI device designed to interface the National Controller Oriented Processor sets with various rotating drum and start-stop printers, as shown in *Figure 1.* It will drive up to 20 parallel print columns, with controls for ribbon color, paper feed, and paper take-up. An additional 4-bit output port provides a 1 kHz tone signal and there are three general purpose outputs under control of the processor.

The MM5788 can also be used as a general purpose I/O chip. In this mode, ten column drivers are outputs and nine function as input/output ports, all under program control.

features

- Capable of driving Seiko Models 102, 104, 210, 220, 101T, 310 and 320 (20 columns)
- Paper feed inhibit for overprinting
- Multiple paper feeds (up to 15)
- Tone output for audio bleep under program control
- Internal power "ON" clear
- Single power supply operation
- TRI-STATE® handshake acknowledge to allow multiple MM5788's and other peripherals to be intermixed for system expansion
- General purpose I/O mode
- On-chip comparators to detect printer timing signals

block diagram



absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All other pins connected to V_{SS})	V_{SS} +0.3V to V_{SS} −12.0V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature	300°C

operating voltage range

$6.5 \le V_{SS} - V_{DD} \le 9.5V$
(V_{SS} is always the most positive supply voltage)

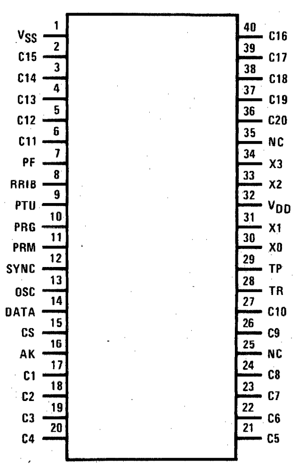
dc electrical characteristics (Ambient Operating Temperature)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Operating Supply Current	T_A = 25°C				
		$V_{DD} = V_{SS} -9.5V$		10		mA
	OSC Input Levels					
V_{IH}	Logical High Level	$V_{DD} = V_{SS} -6.5V$	V_{SS}−0.8			V
		$V_{DD} = V_{SS} -7.9V$	V_{SS}−1.0			V
V_{IL}	Logical Low Level	$V_{DD} = V_{SS} -9.5V$			V_{DD}+1.5	V
	SYNC, DATA, and C2 through C10 Input Levels					
V_{IH}	Logical High Level	$V_{DD} = V_{SS} -6.5V$	V_{SS}−1.0			V
		$V_{DD} = V_{SS} -7.9V$	V_{SS}−1.2			V
V_{IL}	Logical Low Level	$V_{DD} = V_{SS} -9.5V$			V_{SS}−4.0	V
	CS (Chip Select) Input Levels					
V_{IH}	Logical High Level	$V_{DD} = V_{SS} -6.5V$	V_{SS}−2.0			V
		$V_{DD} = V_{SS} -7.9V$	V_{SS}−3.2			V
		$V_{DD} = V_{SS} -9.5V$	V_{SS}−4.2			V
V_{IL}	Logical Low Level	$V_{SS} -9.5V \le V_{DD} \le V_{SS} -6.5V$			V_{DD}+1.0	V
I_{IH}	Input Current	$V_{DD} = V_{SS} -7.9V$				
		$V_{IH} = V_{SS} -3.2V$	−350			µA
	PF, RRIB, PRG, PTU and PRM Output Levels					
I_{OH}	Logical High Level	$V_{OH} = V_{SS} -0.9V$, $V_{DD} = V_{SS} -7.9V$	−0.7			mA
		$V_{OH} = V_{SS} -0.9V$, $V_{DD} = V_{SS} -9.5V$			−3.0	mA
	C1 through C20 Output Levels					
I_{OH}	Logical High Level	$V_{OH} = V_{SS} -0.9V$, $V_{DD} = V_{SS} -7.9V$	−0.7			mA
		$V_{OH} = V_{SS} -0.9V$, $V_{DD} = V_{SS} -9.5V$			−3.0	mA
	T_p, T_r Input Levels					
V_{IH}	Logical High Level		V_{DD}+0.3			V
V_{IL}	Logical Low Level				V_{DD}+0.1	V
	AK Output Levels					
V_{OH}	Logical High Level	$V_{DD} = V_{SS} -6.5V$, $\lvert I_{OH} \rvert < 100\mu A$	V_{SS}−0.9			V
V_{OL}	Logical Low Level	$V_{SS} -9.5V \le V_{DD} \le V_{SS} -6.5V$, $\lvert I_{OL} \rvert < 25\mu A$			V_{SS}+3.7	V
	X0, X1, X2 and X3 Output Level					
I_{OH}	Logical High Level	$V_{OH} = V_{SS} -0.9V$, $V_{DD} = V_{SS} -7.9V$	−0.7			mA
		$V_{OH} = V_{SS} -0.9V$, $V_{DD} = V_{SS} -9.5V$			−3.0	mA
	AK TRI-STATE Outputs					
I_{OH}	Unselected Level	$V_O = V_{SS} -0.5V$, CS = V_{IH}	−10		+10	µA
I_{OL}		$V_O = V_{DD} +0.5V$, CS = V_{IH}	−10		+10	µA
		$V_{SS} -9.5V \le V_{DD} \le V_{SS} -6.5V$				

ac electrical characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_b	Bit Time	*(Figure 5)*	10		12.5	μs
	OSC Duty Cycle	*(Figure 4)*	46	56	66	%
$1/t_p$	OSC Input Frequency	*(Figure 4)*	320		400	kHz
	OSC Input Transition Times	$V_{DD} = V_{SS} - 9.5V$, RC = 0.15μs, *(Figure 4)*				
t_r	Rise Time				350	ns
t_f	Fall Time				50	ns
	SYNC Input Timing	$V_{DD} = V_{SS} - 7.9V$, *(Figure 4)*				
t_{osch}	Hold Time		100			ns
t_{stl}	High-to-Low Set-Up Time		680			ns
t_{sth}	Low-to-High Set-Up Time		100			ns
	CS Input Transition Times	$V_{DD} = V_{SS} - 7.9V$, *(Figure 4)*				
t_r	Rise Time				2.0	μs
t_f	Fall Time				10.0	μs
t_{pdl}	High-to-Low Propagation Time				0.5	μs
t_{pdh}	Low-to-High Propagation Time				2.5	μs
	AK Output Transition Times	$V_{DD} = V_{SS} - 6.5V$, $C_L \leq 100$ pF, *(Figure 5)*				
t_r	Rise Time				1.4	μs
t_f	Fall Time				2.3	μs
t_{pdl}	High-to-Low Propagation Time				3	μs
t_{pdh}	Low-to-High Propagation Time				2.4	μs
	PF, RRIB, PRG, PTU, PRM, TONE, C1–C20 and X1–X3	$V_{DD} = V_{SS} - 6.5V$, $C_L = 100$ pF, $R_{EXT} = 10k$, *(Figure 5)*				
t_r	Rise Time				3	μs
t_f	Fall Time				4.5	μs
t_{pdl}	High-to-Low Propagation Time				4.5	μs
t_{pdh}	Low-to-High Propagation Time				4	μs

connection diagram (Dual-In-Line Package, Top View)



Order Number MM5788N
See Package 24

Pin Descriptions

Inputs

OSC	–	400 kHz input from system oscillator
SYNC	–	SYNC signal input from MM5782
CS	–	A logical low level enables the chip
Data	–	Input for control and data to be printed
TP, TR	–	Inputs for synchronizing pulses from the controlled printer

Outputs

AK	–	Handshake output—functions as "READY" flag. Responds to CS with logical high level if ready to accept data in Printer Control Mode. Operates as serial data output in general purpose I/O mode. TRI-STATE
PF	–	Paper feed control
PTU	–	Paper take up control
PRG	–	Individual paper feed controls for dual tape printers such as the
PRM		Seiko 101T
RRIB	–	Ribbon color control
X0	–	1 kHz Tone Output under program control
X1–X3	–	General purpose latched outputs under program control
C1–C20	–	Column drive outputs (BCD digits 1–20 in command data field)

The PF, PTU, PRG, PRM, RRIB and X0–X3 outputs are controlled by command and operand signals from the MPE of the TCS processor set. *Figure 3* shows a timing example. Table I lists the various instruction codes.

functional description

The MM5788 timing is derived from an external 400 kHz oscillator (OSC) which also drives the MM5781, MM5782 processor. Bit synchronization is attained by using the processor SYNC output together with OSC to generate the 100 kHz internal clocks. All interface signals between the MM5788 and the processor are designed to move on the rising edge of OSC and be sampled on the falling edge of OSC.

PROCESSOR HANDSHAKE

The MM5788 receives commands and data serially from the processor. The handshake sequence is as follows: with timing diagram shown in *Figure 2.*

- The processor drives the Chip Select (CS) line to a logic low level state, enabling the TRI-STATE buffer on the MM5788 acknowledge output (AK).
- The AK output responds with a logic high state if ready to accept data or a logic low state if busy.
- If AK is a logic high state, the processor waits for a start window (logic low state) on the AK line. The window is 4-bits wide and is used to synchronize the internal recirculating registers with the incoming data stream. The wait time is from 1 to 36 bit times.
- Upon detection of the start window, the processor sends a serial data stream on the DATA line. This data stream consists of a start bit (logic high state) followed by a 4-bit command, a 4-bit operand, and up to 80 bits (20 digits) of BCD data. The BCD digits 1–20 correspond to column outputs C1–C20, respectively.
- The MM5788, responding to the start bit, shifts in the next 88 bits from the DATA line, drives AK to a low state, decodes and carries out the action specified by the command. The processor need send only the 4-bit command, the Operand and Data fields are optional.

TABLE I. Instruction Codes for MM5788

INSTRUCTION		CODE		DESCRIPTION
		OPERAND	COMMAND	
Print	MOD 310	1000	OXYZ	X = 0 Print Black
	Others	0000	OXYZ	X = 1 Print Red
				YZ = 00 Feed M, G
				YZ = 01 Feed G
				YZ = 10 Feed M
				YZ = 11 No M,G Paperfeed
Paper Feed		ABCD	10YZ	
Lines Fed				
1		0000		YZ = 00 Feed M,G
15		1000		YZ = 01 Feed G
14		1100		YZ = 10 Feed M
13		1010		YZ = 11 No M,G Feed
12		0111		
11		0100		
10		0110		
9		1101		
8		0011		
7		0010		
6		1011		
5		1110		
4		0001		
3		1001		
2		0101		
1		1111		
Read External				Load C2–C10 serially on to AK
XXXX		dddd	1110	
Reset				
	Model 310, 320	10dd	1111	
	102, 104, 210, 220	01dd	1111	
	101T	11dd	1111	
Load		X3X2X1X0	1100	Load Operand X3X2X1X0 into output latch
		dddd	1101	Load data field into output buffer register

functional description (con'd)

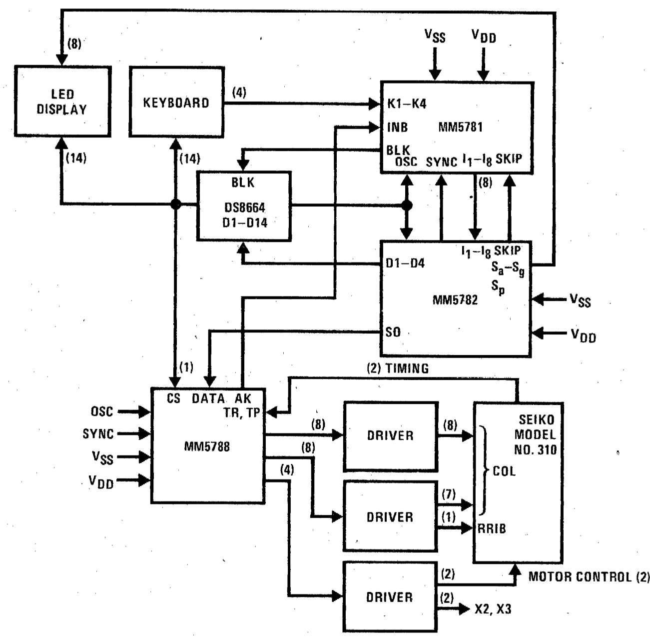


FIGURE 1. Typical Printing Calculator Application

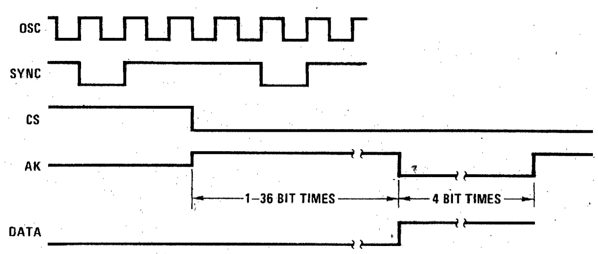


FIGURE 2. Handshake Timing

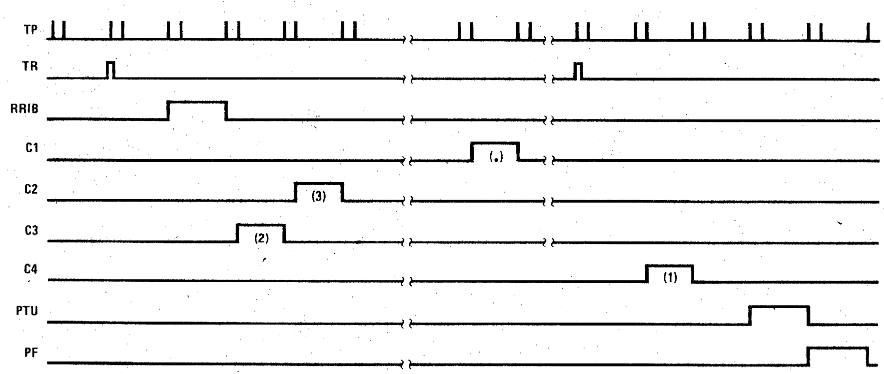
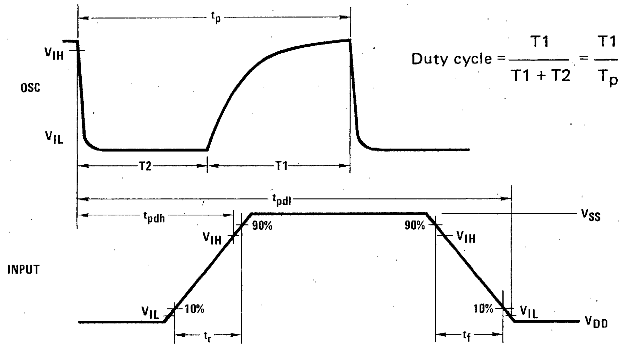


FIGURE 3. Timing Example for Printing 123. in Red on Seiko 102 Printer

functional description (con'd)



$$\text{Duty cycle} = \frac{T1}{T1 + T2} = \frac{T1}{T_p}$$

FIGURE 4. Input Waveform Timing

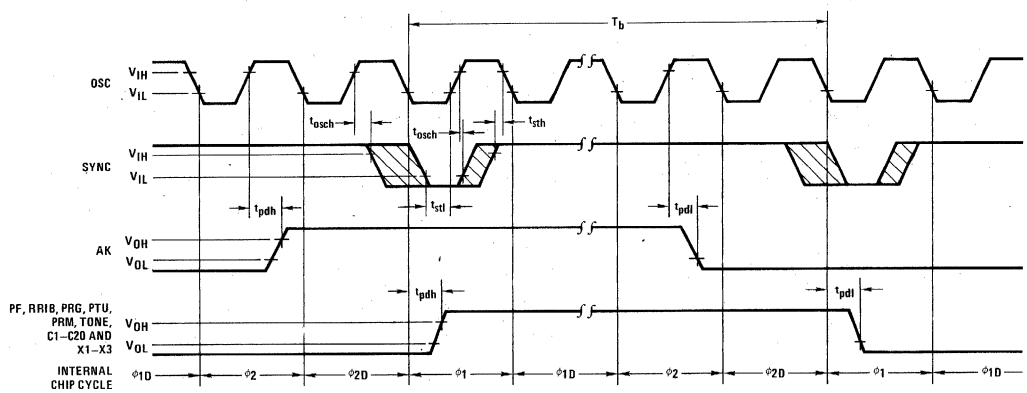


FIGURE 5. Output Waveform Timing

MM5799 Controller Oriented Processor

general description

The MM5799 is an MOS/LSI device containing all system timing, logic, RAM and control ROM functions required for implementation of a Controller Oriented Processor. It is capable of scanning up to 56 keyboard switches or data may be entered as BCD data words. Eight outputs present information in either BCD or 7-segment plus decimal point format and 4 additional latched outputs provide encoded digit timing information. Serial I/O ports allow expansion of the basic 384-bit RAM store and interface to peripheral equipment such as printers. The circuit is capable of being programmed to perform a wide range of customer specified computation and control functions.

features

- 10μs microinstruction cycle time
- 1536 microinstruction ROM (8-bit instruction set)
- 384-bit RAM (96-digit)
- 5 data or control inputs that provide keyboard scanning or BCD inputs
- Internal power on clear with programmable external override
- Serial input and serial output for data storage expansion or interface with a variety of peripheral interface chips
- 3 general purpose input/output lines plus "blanking" output
- 8 fully programmable outputs (7-segment, BCD, etc.)
- Internal or external oscillator
- Single power supply operation
- Direct segment drive of LED's
- Fully compatible with TCS peripheral interface elements and can be programmed to function as a secondary processor element in TCS system

block diagram

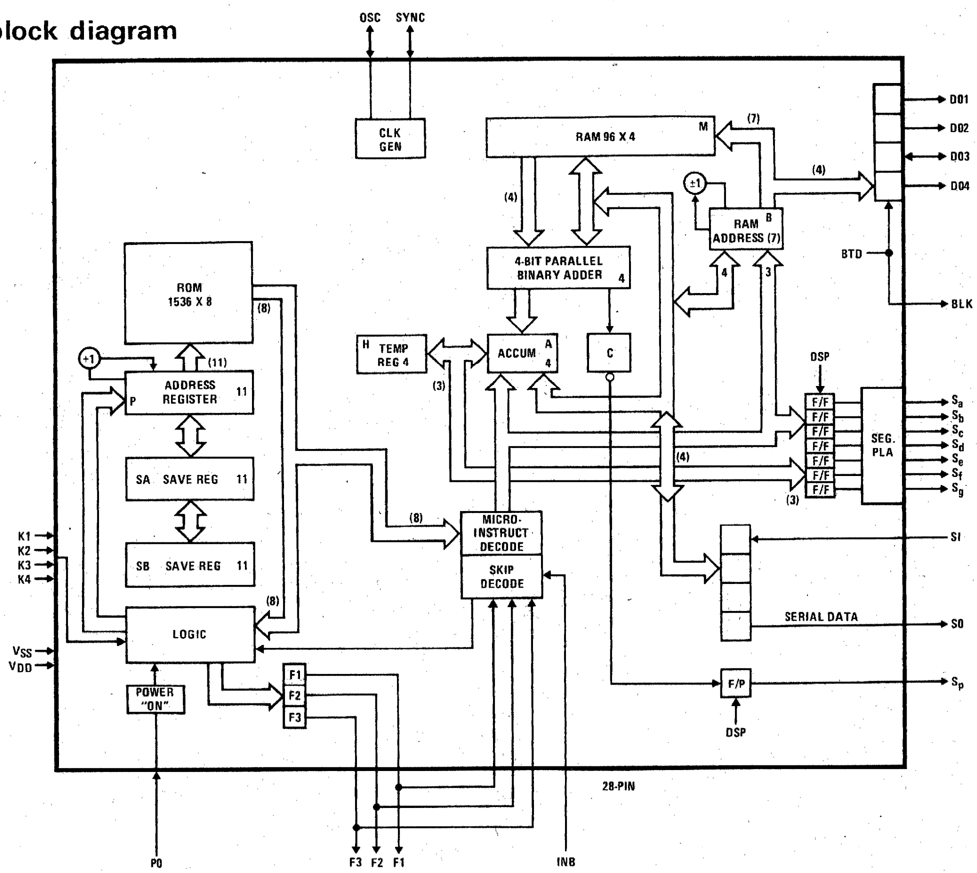


FIGURE 1.

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All Other Pins Connected to V_{SS})	V_{SS} +0.3V to V_{SS} −12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics $0°C \leq T_A \leq +70°C$, $7.9V \leq V_{SS} - V_{DD} \leq 9.5V$ unless otherwise stated

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage ($V_{SS} - V_{DD}$)		7.9		9.5	V
Operating Supply Current (I_{DD})	$V_{SS} - V_{DD}$ = 9.5V, T_A = 25°C (Excluding Outputs)		12	18	mA
Osc Input Voltage Levels					
Logic High Level (V_{IH})	$V_{SS} - V_{DD}$ = 7.9V	V_{SS}−1.0			V
Logic Low Level (V_{IL})	$V_{SS} - V_{DD}$ = 9.5V			V_{DD}+1.5	V
Osc Input Resistance To V_{SS}	Two Options		3		kΩ
			6		kΩ
INB, K1–K4, F1–F3 Input Voltage Levels	(For Keyboard)				
Logic High Level (V_{IH})	$V_{SS} - V_{DD}$ = 7.9V	V_{SS}−3.2		V_{SS}	V
	$V_{SS} - V_{DD}$ = 9.5V	V_{SS}−4.5		V_{SS}	V
Logic Low Level (V_{IL})				V_{DD}+1.5	V
INB, K1–K4 Input Voltage Levels	(As Logic Input)				
Input High Level (V_{IH})		V_{SS}−1.0			V
Input Low Level (V_{IL})				V_{SS}−4	V
INB, K1–K4 Input Current Levels	(Through Keyboard)				
Input High Level (I_{IH})	$V_{IH} = V_{SS}$ − 3.2V			−350	μA
Input Low Level (I_{IL})	$V_{IL} = V_{SS}$ − 32V, Fluorescent Display (See Option 10)	−20			μA
D03 Input Voltage Levels					
Logic High Level (V_{IH})	$7.9V \leq V_{SS} - V_{DD} \leq 9.5V$	V_{SS}−3.5			V
Logic Low Level (V_{IL})	$V_{SS} - V_{DD}$ = 7.9V			V_{DD}+2.5	V
	$V_{SS} - V_{DD}$ = 9.5V			V_{DD}+3.0	V
SI and Sync Input Voltage Levels					
Logic High Level (V_{IH})	$V_{SS} - V_{DD}$ = 7.9V	V_{SS}−1.2			V
Logic Low Level (V_{IL})	$V_{SS} - V_{DD}$ = 7.9V			V_{SS}−4.0	V
D01, D02, D04 Output Voltage Levels (Encoded Digit)					
Logic High Level (V_{OH})	R_L = 150 kΩ	V_{SS}−1.0		V_{SS}	V
Logic Low Level (V_{OL})	I_{OL} = 3μA (If Load Present)	V_{DD}		V_{DD}+0.5	V
Logic High Level Current (I_{OH})	$V_{SS} - V_{DD}$ = 7.9V, $V_{OH} = V_{DD}$ + 1.5V			−260	μA
D03 Output Voltage Levels					
Logic High Level (V_{OH})	R_L = 150 kΩ	V_{SS}−1.0		V_{SS}	V
Logic Low Level (V_{OL})	I_{OL} = 3μA (Load Present)	V_{DD}		V_{DD}+0.5	V
Logic High Level Current (I_{OH})	Battery Low "OFF," from DS8664				
	$V_{OH} = V_{DD}$ + 3V, $V_{SS} - V_{DD}$ = 9.5V	−1.3		−0.3	mA
	$V_{OH} = V_{DD}$ + 2.5V, $V_{SS} - V_{DD}$ = 7.9V	−1.0		−0.4	mA
	Battery Low "ON," from DS8664				
	$V_{OH} = V_{SS}$ − 3V, $V_{SS} - V_{DD}$ = 7.9V			−0.3	mA
	$V_{OH} = V_{SS}$ − 3V, $V_{SS} - V_{DD}$ = 9.5V			−0.4	mA
S_a–S_g and S_p Output Current Levels	(see option 7)				
Logic High Level Current (I_{OH})	$V_{OH} = V_{DD}$ + 3V				
	5 mA Min	−20	−10	−5	mA
	3 mA Min	−12	−6	−3	mA
Logic Low Level Current (I_{OL})	$V_{OL} = V_{DD}$ + 0.5V, (See Option 8)				
	Open Drain	−1		1	μA
	Load Device to V_{DD}	3		15	μA

dc electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S0 and Sync Output Voltage Levels	(With Load and Driver to V_{DD}) $V_{SS} - V_{DD} = 7.9V$				
Logic High Level (V_{OH})	$I_{OH} = -100\mu A$	V_{SS}-0.5		V_{SS}	V
Logic Low Level (V_{OL})	$I_{OL} = 15\mu A$	V_{DD}		V_{DD}+3.7	V
F1, F2, F3 Output Voltage Levels					
Logic High Level (V_{OH})	$I_{OH} = -30\mu A$	V_{SS}-1.5			V
Logic Low Level (V_{OL})	$I_{OL} = 3\mu A$			V_{DD}+1.0	V
Blk Output Voltage Levels					
Logic High Level (V_{OH})	$I_{OH} = -0.5$ mA	V_{SS}-1.5			V
Logic Low Level (V_{OL})	$I_{OL} = 5\mu A$			V_{DD}+1.0	V
Osc Output Current Levels	(Output with Load to V_{DD})				
Logic High Level Current (I_{OH})	$V_{OH} = V_{DD} + 1.5V$			−1.0	mA
Logic Low Level Current (I_{OL})	$V_{OL} = V_{DD} + 0.5V$	3.0			µA
Keyboard Key Resistance (R_{KEY}) (INB, K1–K4, F1–F3)	LED Display Interface			200	Ω
	Fluorescent Display Interface			50	kΩ
INTERFACING WITH MOS					
All Outputs					
Output High Voltage (V_{OH})		V_{SS}-1		V_{SS}	V
Output Low Voltage (V_{OL})	(On-Chip Loads at Outputs)	V_{DD}		V_{DD}+1	V
INB, K1–K4 Input Voltages	(No Input Loads)				
Input High Voltage (V_{IH})		V_{SS}-1		V_{SS}	V
Input Low Voltage (V_{OL})		V_{DD}		V_{SS}-4	V

ac electrical characteristics ($0°C \le T_A \le +70°C$, $7.9V \le V_{SS} - V_{DD} \le 9.5V$ unless otherwise stated)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Osc Input Frequency		320		400	kHz
Osc Duty Cycle *(Figure 2)*		46	56	66	%
Osc Input					
Rise Time (t_r)	$C_L = 25$ pF, $R_L = 6$ kΩ			350	ns
Fall Time (t_f)	RC = 0.15µs			50	ns
Sync Input Timing					
Interval (t_B, Bit Time)		10		12.5	µs
Low Hold Time (t_{OXH})		100			ns
High Hold Time (t_{OSCH})		100			ns
Low Set-Up Time (t_{STL})		680			ns
High Set-Up Time (t_{STH})		100			ns
K1–K4, INB, F1–F3, D03 Input Timing					
t_{SK}		1.75			µs
t_{LK}		1.0			µs
SI Input Timing					
t_{SX}		1.5			µs
t_{HLDX}		0.5			µs
BLK Output Timing					
t_{pdBLK}	$C_{LOAD} = 50$ pF			4.4	µs
t_{rb}	$C_{LOAD} \le 20$ pF	0.3			µs
F1, F2, F3 Output Timing	$C_{LOAD} = 100$ pF			4.4	µs
t_{pdf}					
Osc Output Frequency		130		450	kHz
Osc Output Duty Cycle		33	56	68	%
Sync Output Timing					
Interval (t_B, Bit Time)	(For On-Chip Oscillator)	8.8		30	µs
t_{pdsL}	$C_L = 250$ pF	0.1		1.65	µs
t_{pdsH}		0.1		1.25	µs
t_{HS}		0.1		0.8	µs
D01, D02, D03, D04, S0 Output Timing	$C_L = 100$ pF (D01–D04) $C_L = 250$ pF (S0)				
t_{pd}		0.5		4.0	µs
S_a–S_g, S_p Output Timing (t_{pdSEG})				6.0	µs
Interdigit Blanking Time (T1)				7.5	µs

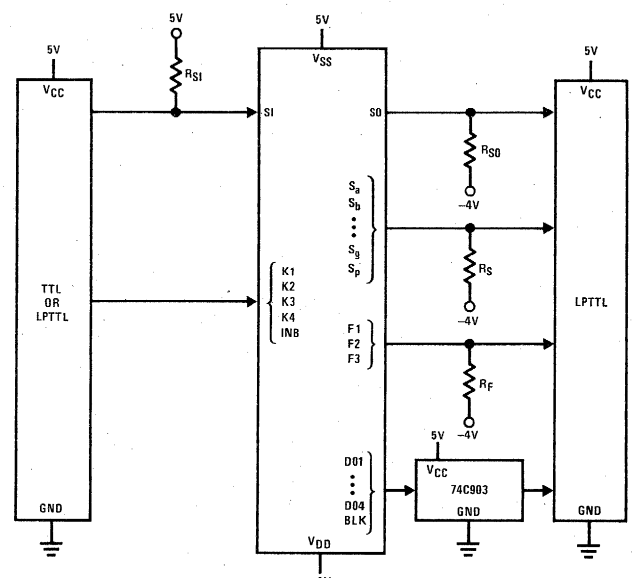
options

In addition to internal programming, for various applications, the following input/output options increase flexibility of the MM5799 for both calculator and other computational operations.

1) On-chip oscillator with oscillator output or external oscillator with on-chip load resistor (6 kΩ or 3 kΩ to V_{SS})
2) SYNC pin an output or input. The SYNC pin defines the beginning of an internal cycle time, ϕ_1, during coincidence of low levels on OSC and SYNC, as shown in *Figures 2(a) and 2(b).*
3) DO3 can be an output, an input or both.
4) RAM can be organized as 8 registers of 12 digits or 6 registers of 16 digits.
5) The shift register can be organized in either of the following two modes:
   i) Data is shifted continuously from SI through a 4-bit register to SO. An AXO instruction exchanges contents of register A with contents of shift register. The lowest order bit is shifted out on SO.
   ii) The input of the shift register is tied to one. AXO inputs SI to the most significant bit of A and A is shifted out of SO. Therefore, SI can be an input which does not affect SO.
6) The EXC+ instruction can be modified not to skip on B going to 13.
7) Segment outputs can be programmed for a minimum source current of 3 mA or 5 mA.
8) All outputs may be open drain or have a load device to V_{DD}. In addition SO may also have an active driver to V_{DD}.
9) Power-on-reset may be brought in as an external reset pin.
10) The K inputs and INB may be active high or active low. The switching levels can be set for a keyboard or for a logic input. Input loads can go to V_{SS}, V_{DD} or be absent. And the inputs can be made to withstand −35V for interfacing with fluorescent displays.
11) The decodes of the BCD to segment PLA are mask-programmable for any characters (except 8).

TTL interface

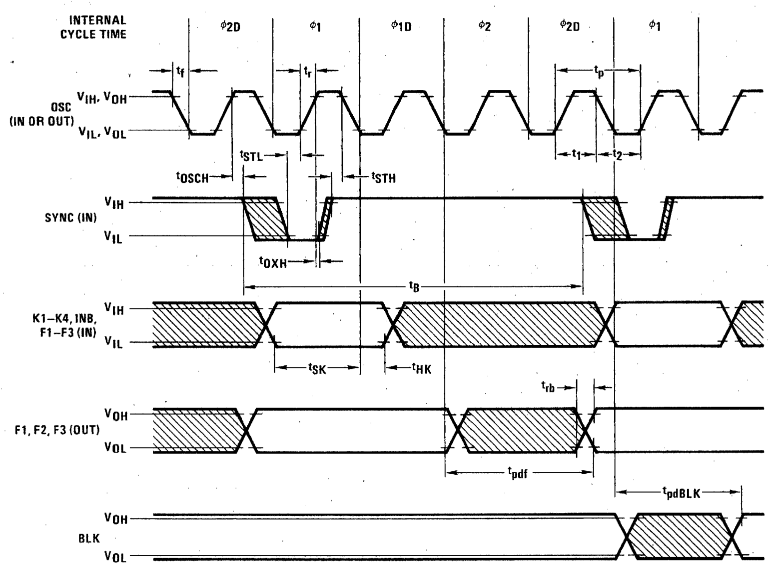
The MM5799 can interface with LPTTL with the external components shown below. The MM5799 outputs source current to provide a "1" level to LPTTL and external resistors must be provided to sink current for a "0" level. When driving the MM5799 from LPTTL an on-chip load to V_{SS} on the K inputs and INB insure a proper high level. An external resistor to V_{SS} must be supplied on the SI input to overcome a load device to V_{DD} on that pin.



8.4 kΩ is the maximum resistor that will still sink one LPTTL load and the lower resistor value still allows a 2.7V "1" level for R_{SO}, R_{S1} and R_F. R_F of 2.8k will overcome the device on SI and 680Ω is the minimum resistor that LPTTL can sink.

$670\Omega \le R_{SI} \le 2.81\ k\Omega$
$3.5\ k\Omega \le R_{SO} \le 8.4\ k\Omega$
$1.9\ k\Omega \le R_S \le 8.4\ k\Omega$
$4.6\ k\Omega \le R_F \le 8.4\ k\Omega$

switching time waveforms



Note. OSC Duty Cycle = $\dfrac{t_1}{t_1 + t_2} = \dfrac{t_1}{t_p}$

FIGURE 2(a). Input/Output Timing Diagram (External SYNC)

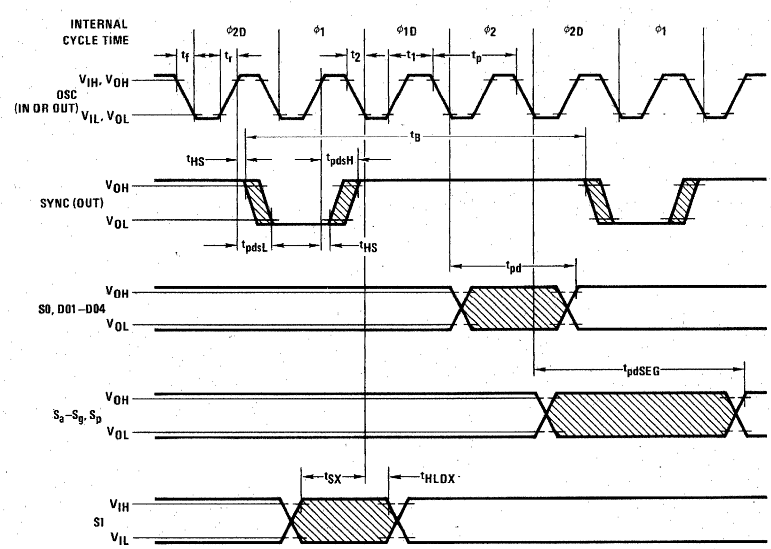
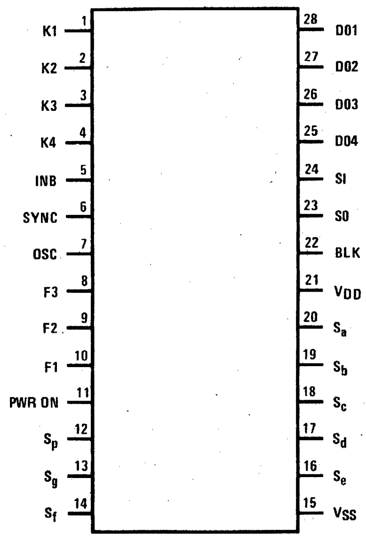


FIGURE 2(b). Input/Output Timing Diagram (Internal SYNC)

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5799N
See Package 23

functional description

A block diagram of the MM5799 is shown in *Figure 1.* The control ROM is organized as 1,536 8-bit instruction words. ROM addressing is by an 11-bit Program Counter Register P and 2 push-down address save registers, SA and SB. Internal data flow, storage, and input/output lines are controlled by 8-bit ROM instruction words.

Arithmetic and logic functions are performed in the 4-bit adder with results stored in accumulator A.

The RAM contains 384 bits, addressed as 96 4-bit words. Register lengths are under program control; e.g., the memory can be formatted as 6 registers x 16 digits, 8 registers x 12 digits.

Seven outputs are decoded by the segment PLA and brought out as either BCD or 7-segment information depending on the software program. Decimal position is brought out on the S_P line. The segment and decimal point output buffers are capable of driving LED displays directly. Digit timing information for driving displays and external keyboard scanning is encoded into a 4-bit code and brought out on the digit output lines D01–D04 and used by the DS8664, DS8665, DS8666, DS8881 or DS8882 Decoder/Drivers to generate up to 14 digit outputs. A 2-bit code is used in systems employing the DS8874 Decoder/Driver *(Figures 4 and 5).*

Serial input and output ports (SI and SO) are provided for accessing external RAM and interfacing with peripheral equipment such as printers.

4 K-inputs may be used for direct data inputs or as key inputs scanned by 14 externally decoded digit output lines (D01–D04) for up to 56-key keyboards. There are 3 additional general purpose latched input/output ports, F1–F3. The BLK output is used as a blanking signal for the digit decoder/driver. One general purpose input INB can be tested under program control.

The MM5799 has an internal power-on clear which is initiated when the V_{DD} supply has reached a nominal value of V_{SS}–6V. The power-on clear is then extended for an additional 1 ms. External power-on clear can be provided which will override the internal clear when power supply turn-on time is not within the design specification of the MM5799, see Options, no. 9.

register and I/O port definitions

DESCRIPTIONS	DESIGNATIONS
12,288-bit Control ROM 1,536 words x 8 bits (24 pages of 64 words)	I_8–I_1
11-bit Program Register Page P_p (P11 – P7) Word P_w (P6 – P1)	P
2 x 11-bit Program Address Save Registers	SA, SB
384-bit RAM organized as 8 registers x 12 digits x 4 bits (r x d x z) or 6 x 16 x 4	M
7-bit RAM Address Register Register B_r (B7 – B5) Digit B_d (B4 – B1)	B
4-Bit Accumulator	A
4-bit Holding Register	H
1-bit Carry Register	C
4 Data or Control Inputs	K1–K4
3 General Purpose Programmable Input/Output Lines	F1–F3
8 Latched Programmable Outputs (S_a–S_d available as BCD under program control)	S_a–S_g, S_p
General Purpose Input	INB
4 Latched Digit Outputs	DO4–DO1
Serial Input and Output Ports	SI and SO
Blanking Signal Output	BLK

standard instructions

	MNEMONIC	DATA FLOW	SKIP IF	DESCRIPTION
Arithmetic Operations	AD	M + A → A		Add M (B) to A, store sum in A
	ADD	C + M + A → A		Add carry bit to M (B). Add sum to A, store sum in A
		1 → C if A ≥ 10 0 → C if A < 10	A < 10	Set C if A ≥ 10, reset C if A < 10
	SUB	M + $\bar{A}$ + C → A		Subtract A from M
		Overflow → C	Overflow	Overflow to C
	COMP	$\bar{A}$ → A		One's complement of A to A
	OTA	0 → A		Clear Accumulator
	ADX (Y)	A + Y → A	No overflow and Y ≠ 6	Add constant (Y) to A. Store sum in A. Y = 1, 2 . . . 15
	HXA	H ↔ A		Exchange contents of H register with A
	TAM		A = M (B)	Compare contents of A to M (B), skip if A = M (B)
	SC	1 → C		Set C register
	RSC	0 → C		Reset C register
	TC		C = 0	Skip if C = 0
Input Test	TIN		INB = 1	Test INB. Active state of input is programmable
	TF (N)		F (N) = 0	Test F (N) pin. N = 1, 2, 3
	TKB		K = 1	Skip if any K input active. Active state of input is programmable
	TIR		DO3 = 0	Test DO3 pin as input

standard instructions (con't)

	MNEMONIC	DATA FLOW	SKIP IF	DESCRIPTION
Input/Output	BTD	$\overline{B_d} \rightarrow$ DO4 – DO1		Transfer contents of B_d to digit output latches, turns BLK output low for one cycle time
	DSPA	$A \rightarrow S_a - S_d$ $H \rightarrow S_e - S_g$ $\overline{C} \rightarrow S_p$		A4 – A1 to output latches, directly to outputs $S_a - S_d$. H3 – H1 to output latches, direct to $S_e - S_g$. $\overline{C}$ to S_p latch
	DSPS	$A \rightarrow S_a - S_g$ $\overline{C} \rightarrow S_p$		A to output latches, 7-segment decoded to $S_a - S_g$. Segment decode is programmable. $\overline{C}$ to S_p latch
	AXO	$SI \rightarrow A$ $A \rightarrow SO$		Exchange accumulator with serial input/output
	LDF	If $\overline{I_6^*}:\overline{I_5^*} \rightarrow F3$ If $\overline{I_4^*}:\overline{I_3^*} \rightarrow F2$ If $\overline{I_2^*}:\overline{I_1^*} \rightarrow F1$		N = 1, 2, 3. Load F (N) from next instruction word. 2 microcycle instruction
	READ	K4 – K1 $\rightarrow$ A		Read K inputs to A. Active state of input is programmable
Control Functions	GO TO (GO)	$I_6 - I_1 \rightarrow P_W$ If Pp = 1111 X : 11110 $\rightarrow$ Pp		Load next ROM instruction address If on page 36_8 or 37_8 reset page address to 36_8 (Note 1)
	CALL	$I_6 - I_1 \rightarrow P_W$, IIIII $\rightarrow$ Pp If Pp $\neq$ IIIIX : SA $\rightarrow$ SB, P + 1 $\rightarrow$ SA		Call subroutine. If not on page 36_8 or 37_8, push down address save registers. Set page address to 37_8
	RET	SA $\rightarrow$ P SB $\rightarrow$ SA, SB $\rightarrow$ SB		Pop up ROM address save registers
	RETS	SA $\rightarrow$ P SB $\rightarrow$ SA, SB $\rightarrow$ SB	SKIP	RET, then skip next instruction upon return
	LG/GO	Load P $\overline{I_4} - \overline{I_1}, I_8^* \rightarrow P_p$ $I_6^* - I_1^* \rightarrow P_W$		2 microcycle operation. Long GO TO, Load Pp and P_W (Note 1)
	LG/CALL	SA $\rightarrow$ SB, P + 1 $\rightarrow$ SA Load P		2 microcycle operation. Long call. Load Pp and P_W. Push down address save register (Note 1)
	NOP			No operation
Memory Digit Operations	EXC (r)	A $\leftrightarrow$ M (B) $B_r \oplus r \rightarrow B_r$		Exchange data word at M (B) with A. EXCLUSIVE-OR B_r with r. r = 0, 1, 2, 3
	EXC –(r)	A $\leftrightarrow$ M (B) $B_r \oplus r \rightarrow B_r$, $B_d - 1 \rightarrow B_d$	$B_d \rightarrow 15$	Exchange and decrement B_d EXCLUSIVE-OR B_r with r. r = 0, 1, 2, 3
	EXC +(r)	A $\leftrightarrow$ M (B) $B_r \oplus r \rightarrow B_r$, $B_d + 1 \rightarrow B_d$	$B_d \rightarrow 0$ or $B_d \rightarrow 13$	Exchange and increment B_d EXCLUSIVE-OR B_r with r. r = 0, 1, 2, 3
	MTA (r)	M (B) $\rightarrow$ A $B_r \oplus r \rightarrow B_r$		Load accumulator with data word M (B) EXCLUSIVE-OR B_r with r. r = 0, 1, 2, 3
	LM (Y)	Y $\rightarrow$ M (B) $B_d + 1 \rightarrow B_d$		Load memory with Y. Y = 0, 1, 2, . . .15 Increment B_d
Memory Bit Operations	SM (Z)	1 $\rightarrow$ M (B, Z)		Set Bit Z of M (B), Z = 1, 2, 4, 8
	RSM (Z)	0 $\rightarrow$ M (B, Z)		Reset Bit Z of M (B)
	TM (Z)		M (B, Z) = 0	Test Bit Z of M (B), skip if 0
Memory Address Operations	LB (r, d)	$r \rightarrow B_r, d \rightarrow B_d$		r = 0, 1, 2, 3. d = 0 , 11, 12, 13, 14, 15. Load B register. Successive LB's are ignored (Note 2)
	LBL	$I_7^* - I_5^* \rightarrow B_r$, $I_4^* - I_1^* \rightarrow B_d$		2 microcycle instruction. Load next ROM word into B register
	ATB	$A \rightarrow B_d$		Transfer contents of accumulator to B_d register
	BTA	$B_d \rightarrow A$		Transfer contents of B_d register to accumulator
	HXBR	$H \leftrightarrow B_r$		Exchange contents of H and B_r registers

Note 1: ROM pages 10_8 through 17_8 cannot be used.

Note 2: d = 4, 11, 12, 13, 14, 15 when RAM is configured 8 x 12 x 4.

*Second microcycle word

operation codes

OP CODE				MNEMONIC			
$I_8 I_7$	$I_6 I_5$	$I_4 I_3$	$I_2 I_1$	00	01	10	11
00	XX	00	00	NOP	DSPA	COMP	0TA
00	XX	00	01	HXBR	DSPS	AXO	HXA
00	XX	00	10	ADD	AD	SUB	TAM
00	XX	00	11	SC	LBL	RSC	LDF
00	XX	01	00	TF1	TF2	TF3	READ
00	XX	01	01	TIR	TKB	BTD	TIN
00	XX	01	10	MTA (r)			
00	XX	01	11	EXC (r)			
00	XX	10	00	EXC– (r)			
00	XX	10	01	EXC+ (r)			
00	XX	10	10	LB (r, 0)*			
00	XX	10	11	LB (r, 11)			
00	XX	11	00	LB (r, 12)			
00	XX	11	01	LB (r, 13)			
00	XX	11	10	LB (r, 14)			
00	XX	11	11	LB (r, 15)			
01	00	00	XX	RET	RETS	RSM (8)	BTA
01	00	01	XX	TM (1)	TM (2)	TM (4)	TM (8)
01	00	10	XX	RSM (1)	SM (1)	SM (8)	RSM (4)
01	00	11	XX	RSM (2)	TC	SM (2)	SM (4)
01	01	00	XX	ATB	ADX (1)	ADX (2)	ADX (3)
01	01	01	XX	ADX (4)	ADX (5)	ADX (6)	ADX (7)
01	01	10	XX	ADX (8)	ADX (9)	ADX (10)	ADX (11)
01	01	11	XX	ADX (12)	ADX (13)	ADX (14)	ADX (15)
01	10	00	XX	LG (36, 37)	LG (35, 34)	LG (33, 32)	LG (31, 30)
01	10	01	XX	LG (27, 26)	LG (25, 24)	LG (23, 22)	LG (21, 20)
01	10	10	XX	LG (17, 16)	LG (15, 14)	LG (13, 12)	LG (11, 10)
01	10	11	XX	LG (7, 6)	LG (5, 4)	LG (3, 2)	LG (1, 0)
01	11	00	XX	LM (0)	LM (1)	LM (2)	LM (3)
01	11	01	XX	LM (4)	LM (5)	LM (6)	LM (7)
01	11	10	XX	LM (8)	LM (9)	LM (10)	LM (11)
01	11	11	XX	LM (12)	LM (13)	LM (14)	LM (15)
10	XX	XX	XX	CALL			
11	XX	XX	XX	GO			

*Programmable 0 — 10.

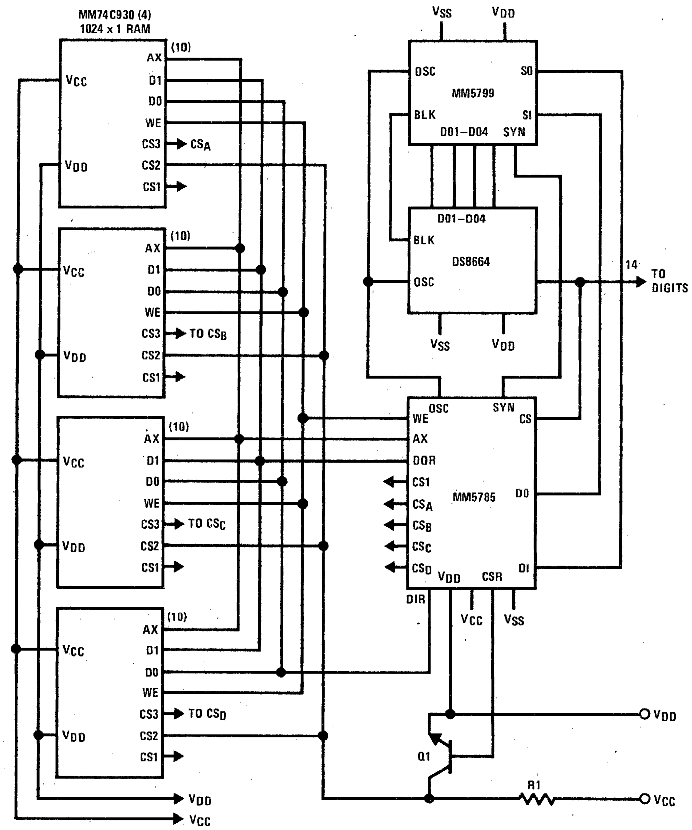
applications information

Versatility of the MM5799 is enhanced by the availability of circuits to interface the chip with a variety of drum printers, displays, and additional read/write store.

The MM5785 RAM Interface Element allows expansion of the on-chip 384-bit store using 1024 x 1-bit random access memory chips. *Figure 3* illustrates the technique used to interface the MM5799 to additional RAM such as might be required in a low-cost electronic cash register system. Low power CMOS memory is used with battery standby power available for retention of totals during periods of power interruption. MM2102 RAMs may be used for low-cost storage when power is not critical.

The MM5788 Printer Interface Element provides the logic and control functions necessary to operate a Seiko Model 101, 102, 104, 210, 310 or 320 type printer from the MM5799. DS8863A transistor buffers are used as current amplifiers between the MM5788 and printer. A typical application of the MM5799 in a printing calculator is illustrated in *Figure 4.* The MM5788 is also useful as a data interface element providing 9 I/O pins and 12 output ports.

applications information (con't)



Note. Q1 and R1 are required only if the RAMs are operated on battery during system power "OFF."

FIGURE 3. MM5799 with Expanded RAM

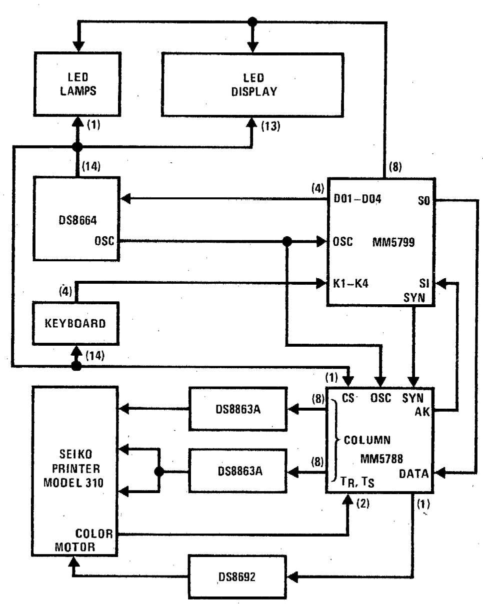


FIGURE 4. Printing and Display Calculator

applications information (con't)

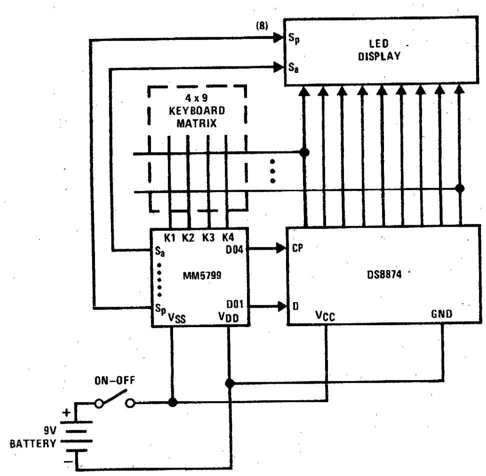


FIGURE 5. Low Cost 9-Digit Calculator Using MM5799

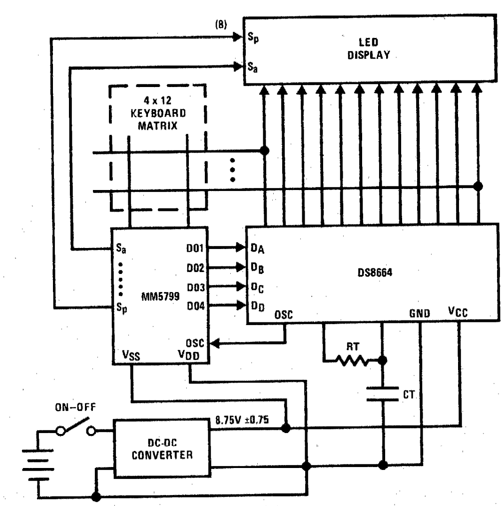


FIGURE 6. Low Cost Scientific Calculator Using MM5799

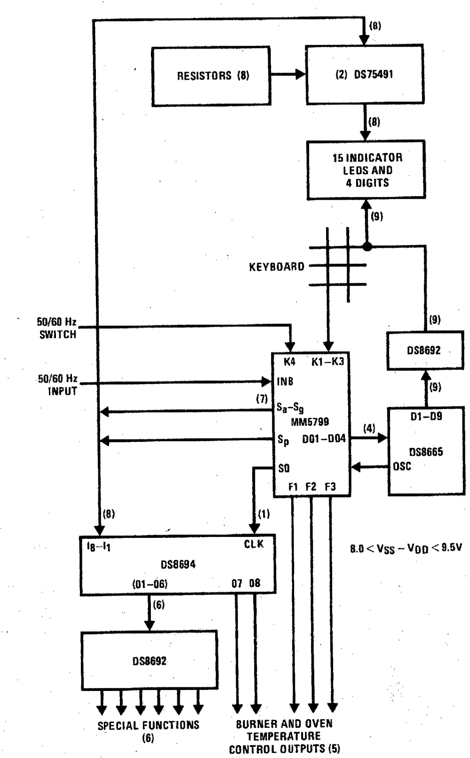


FIGURE 7. Oven Timing and Control System

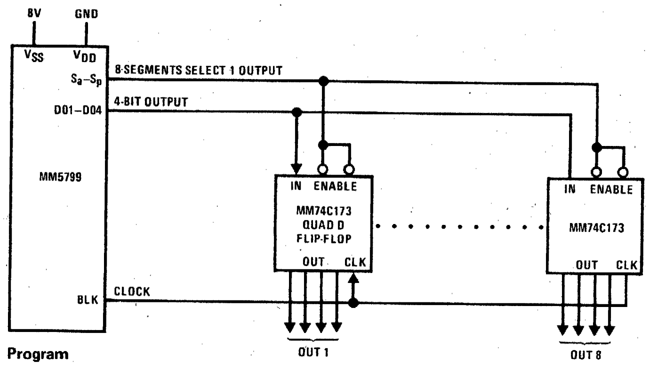
There are 6-digit decoder/drivers that can be used with the MM5799 in LED systems. Three are actually the same basic bipolar chip with different metal mask options. The DS8664 is the decoder for low power, battery operated applications. It supplies 1 of 14 outputs decoded from the 4 bits of encoded timing information generated by the MM5799. The active output state sinks at least 80 mA of driving current at each of its 14 digit outputs. The DS8665 is similar, but has inverted outputs that source 8 mA of current and is used in conjunction with DS8692 transistor arrays for large LED displays with high current requirements. The DS8666 is used in special applications which require only 8 digits or less of high current display, but need all 14 digits out to scan keyboards or address extra data storage. It has 8 current sourcing digit outputs and 6 sinking type outputs. An output enable signal can be used to blank the outputs of the drivers during input transition periods to eliminate any timing "glitches" at the outputs or reduce power dissipation of the system during shut-down mode. The DS8664 has an on-chip 3-cell battery voltage sensing circuit which signals a low battery condition back to the MM5799 through the D03 input. The fourth decoder/driver that can be used is the DS8874. It is useful for very low-cost handheld calculators as shown in *Figure 6*. The DS8881, DS8882 are similar to the DS8664, but have active high outputs to drive vacuum fluorescent grids (digits).

An on-chip oscillator is available for applications in which frequency variations are not critical. An oscillator also exists on the DS8664, DS8665, DS8666, DS8881, and DS8882 Decoder/Driver and can be used for more critical applications. An external timing resistor and capacitor provides more accurate setting of oscillator frequency.

applications information (con't)

Application of the MM5799 as an oven timing and control system is illustrated in *Figure 7.* The controller derives timing signals from a 50 or 60 Hz line and displays time of day in the "idle" mode. The chip stores turn-on time, turn-off time and temperature for each of 4 burners and the oven. Six special function outputs are provided for control of lights, fans, etc. This application illustrates the use of the MM5799 in the general area of control processors. The DS8694 has clocked input latches which allow the segment outputs of the MM5799 to be used as both control and display ports on a time multiplexed basis.

Figures 8 and 9 show some example methods of expanding I/O and control for general controller applications.



Program

Set-up A, H, C DSPA	Output 1 of 8 Select
Set-up B BTD	Output 4-Bit Data

FIGURE 8. 8 Output Groups of 4 Each

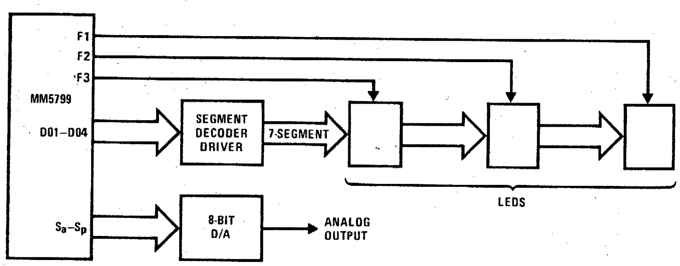


FIGURE 9. Multiplexed Display and 8-Bit D/A

MM57109 number processing unit

general description

The MM57109 is an MOS/LSI digit-oriented microprocessor intended for use in number processing applications. Scientific calculator functions, test and branch capability, internal data storage, and general purpose input/output ports have been combined in this single chip device. Programming is done in calculator keyboard level language with software development simplified and generated code more reliable because algorithms are preprogrammed in an on-chip ROM. Data or instructions can be synchronous or asynchronous; digit count, calculation mode, error control are user programmable; a sense input and flag outputs are available for single bit control.

The MM57109 can be used as a stand alone processor with external ROM/PROM and program counter (PC). Alternatively, it can be configured as a peripheral device on the bus of a microprocessor or minicomputer.

features

Scientific calculator instructions (RPN)

- Floating point or scientific notation
- Up to 8-digit mantissa, 2-digit exponent
- 4-register stack, 1 memory register
- Trigonometric functions, logarithmic functions, Y^X, e^X, π, etc.
- Error flag generation and recovery

Flexible input/output

- HOLD input allows asynchronous instructions, single step, DMA stall
- Asynchronous digit input instruction (AIN) with AIN ready ($\overline{ADR}$) input
- Multi-digit I/O instructions (IN, OUT)
- Programmable mantissa digit count
- Sense input and flag outputs

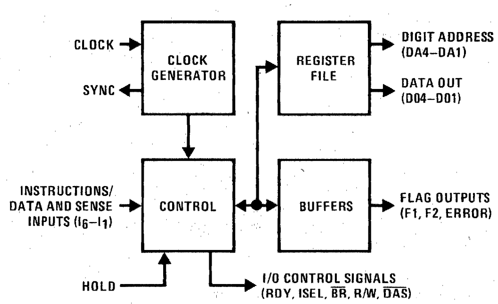
Branch control

- Conditional and unconditional program branching
- Increment/decrement skip on zero for program loops

Interface simplicity

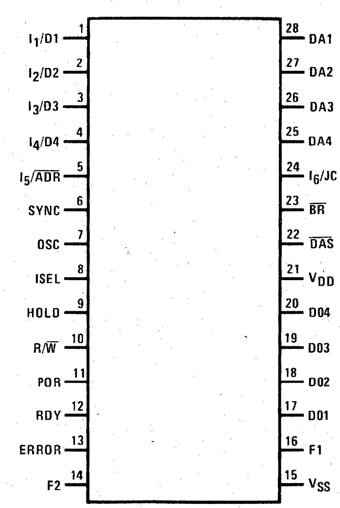
- Single ϕ clock
- Low power operation
- Generation of I/O control signals
- Separate digit input, output, and address bus

block diagram



connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM57109N
See Package 23

COPS

MM57126 COPS memory

general description

The MM57126 is a 1024-bit shift register designed to directly interface with National's MM5782 and MM5799 Controller Oriented Processors. The device is configured as sixteen 64-bit registers with address decoding and control logic to perform the handshake sequence and to synchronize the MM57126 timing with the controlling processor. A chip select input allows up to fourteen MM57126 registers to be used with a single processor when the decoded digit lines are used as chip select drive.

features

- Direct interface to MM5782 and MM5799 for RAM expansion
- Chip select input for multiple MM57126 system usage

block diagram

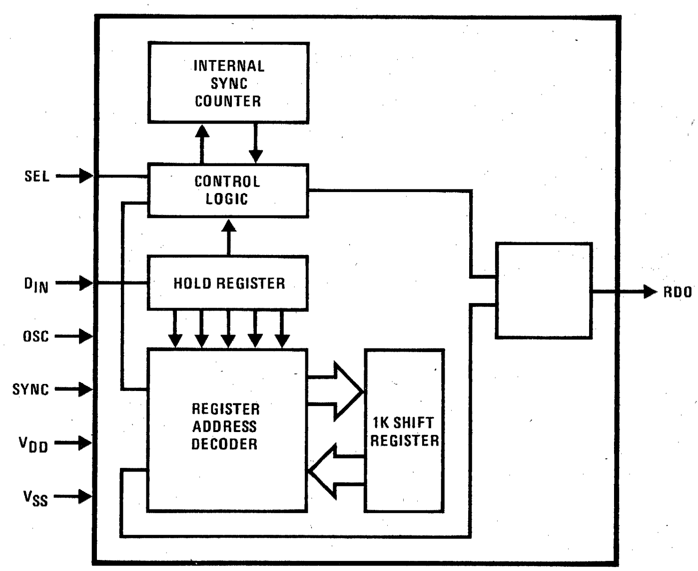


FIGURE 1. MM57126 1K Shift Register Element

connection diagram

Dual-In-Line Package

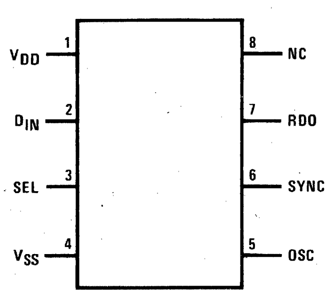


FIGURE 1a.

Order Number MM57126N
See Package 17

Pin Description

OSC	–	Oscillator input
SYNC	–	SYNC input from Controller Oriented Processor
SEL	–	Chip select line input. Active at logical low level (V_{DD})
D_{IN}	–	Data input from Controller Oriented Processor (SO).
RDO	–	Output to Controller Oriented Processor (SI). RDO is active logical low level (V_{DD}) when chip is ready. During read command data stream flows out of MM57126.
V_{SS}	–	Positive power supply terminal. $6.5V \leq V_{SS} - V_{DD} \leq 9.5V$
V_{DD}	–	Negative power supply terminal. $6.5V \leq V_{SS} - V_{DD} \leq 9.5V$.

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All Other Pins Connected to V_{SS})	V_{SS} + 0.3V to V_{SS} − 12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$-6.5V \geq V_{SS} - V_{DD} \geq -9.5V$

(V_{SS} is always the most positive supply voltage)

dc electrical characteristics (0°C to +70°C except where noted otherwise)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current (I_{DD})	$V_{DD} = V_{SS} - 9.5V$, $T_A = 25°C$		12	20	mA
OSC Input Levels					
Logic High Level (V_{IH})	$V_{DD} = V_{SS} - 6.5V$	V_{SS}−1.0			V
Logic High Level (V_{IH})	$V_{DD} = V_{SS} - 7.9V$	V_{SS}−1.0			V
Logic Low Level (V_{IL})	$V_{DD} = V_{SS} - 9.5V$			V_{DD}+1.5	V
SYNC and D_{IN} Input Levels					
Logic High Level (V_{IH})	$V_{DD} = V_{SS} - 6.5V$	V_{SS}−1.2			V
Logic High Level (V_{IH})	$V_{DD} = V_{SS} - 7.9V$	V_{SS}−1.2			V
Logic Low Level (V_{IL})	$V_{DD} = V_{SS} - 7.9V$			V_{SS}−4.0	V
SEL Input Levels					
Logic High Level (V_{IH})	$V_{DD} = V_{SS} - 6.5V$	V_{SS}−2.5			V
	$V_{DD} = V_{SS} - 7.9V$	V_{SS}−3.2			V
	$V_{DD} = V_{SS} - 9.5V$	V_{SS}−4.5			V
Logic Low Level (V_{IL})	$V_{SS} - 9.5 \leq V_{DD} \leq V_{SS} - 7.9V$			V_{DD}+1.5	V
	$V_{DD} = V_{SS} - 6.5V$			V_{DD}+0.4	V
High Level Current (I_{IH})	$V_{IH} = V_{SS} - 3.2V$ $V_{DD} = V_{SS} - 7.9V$			−350	µA
High Level Current (I_{IH})	$V_{IH} = V_{SS} - 2.5$ $V_{DD} = V_{SS} - 6.5V$			−350	µA
RDO Output Levels					
Logic High Level (V_{OH})	$I_{OH} \leq -100\ \mu A$ $6.5 \leq V_{SS} - V_{DD} \leq 9.5$	V_{SS}−0.5			V
Logic Low Level (V_{OL})	$I_{OL} \geq 25\ \mu A$				
	$V_{DD} = V_{SS} - 6.5V$			V_{DD}+2.5	V
	$V_{SS} - 9.5 \leq V_{DD} \leq V_{SS} - 7.9$			V_{DD}+3.7	V

ac electrical characteristics (0°C to +70°C except where noted otherwise)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Bit Time (t_B)		10		50	μs
OSC Input Frequency		80		400	kHz
OSC Duty Cycle	*(Figure 5)*	46	56	66	%
T1		1.1			μs
T2	OSC Frequency = 400kHz	0.85			μs
SYNC Input Transition Times					
Rise Time (t_r)				0.5	μs
Fall Time (t_f)				1.0	μs
OSC Input Transition Time					
Rise Time (t_r)	OSC Frequency = 400kHz			330	ns
Fall Time (t_f)				50	ns
SYNC Input Set-Up Times					
$t_{SET\text{-}UP}$ to V_{IL}	*(Figure 5)*			2.0	μs
$t_{SET\text{-}UP}$ to V_{IH}				0.0	μs
D_{IN} Input Transition Times					
Rise Time (t_r)				1.2	μs
Fall Time (t_f)				2.2	μs
D_{IN} Input Set-Up Times					
$t_{SET\text{-}UP}$				2.5	μs
t_{HOLD}	*(Figure 4)*	3.5			μs
SEL Input Transition Times					
t_r				2.0	μs
t_f				0.1	μs
SEL Input Set-Up Times					
$t_{SET\text{-}UP}$				2.5	μs
t_{HOLD}	*(Figure 4)*	3.5			μs
RDO Output					
t_r	$C_L \leq 100$ pF			2.0	μs
t_f	$V_{DD} = V_{SS} - 6.5V$			2.0	μs
t_{pdH}	$V_{DD} = V_{SS} - 7.9V$, *(Figure 4)*			3.5	μs
t_{pdH}	$V_{DD} = V_{SS} - 6.5V$, *(Figure 4)*			5.5	μs
t_{pdL}	$V_{DD} = V_{SS} - 6.5V$, *(Figure 4)*			3.5	μs
t_{pdL1}	$V_{DD} = V_{SS} - 7.9V$, *(Figure 4)*			4.0	μs

functional description

The chip is configured as sixteen 64-bit shift registers, with appropriate address decoding and control logic to perform the handshaking sequence and synchronize the MM57126 timing with the controlling processor.

The processor must generate a start bit first, then 16 write commands to clear the MM57126 on power "ON". *Figure 2* shows a typical system configuration using multiple MM57126's for RAM expansion.

functional description (Continued)

The MM57126 communicates serially with the processor. The handshake sequence is *(Figure 3)*:

a) The processor drives the chip select (SEL) line to a logical low level state.

b) The ready output (RDO) responds with a logical low level when MM57126 is ready to communicate.

c) For a valid handshake, the D_{IN} input should be at logical low level during ready transition, and the MM57126 should receive the start bit within 3 to 12-bit times from the ready transition; else the ready output is reset and the processor has to wait (if SEL is still at low level) for the next ready.

d) During a valid handshake, the data stream consists of: a start bit, a read/write bit, a 4-bit Delay, 4 register address bits and 64-bits of data as shown in *Figure 3a*. Data flows serially in or out of the MM57126, depending on the read/write command.

e) Handshaking terminates when the ready signal goes back to a logic high level.

The Controller Oriented Processor can be programmed to generate the following assembly language routine for expanding data storage using one or more MM57126's.

MAIN PROGRAM

(i) **Write:** Write register 0 of processor to register N on the selected chip Y.

	Instruction	Comments
	LB 2, 15	
	LM N	Load register address N into M (2, 15). (N = 0, 1, 2, . . . 15.)
	LBL 0, Y	Load B register of processor with MM57126 chip address Y. (Y = 1, 2, . . . 14).
	CALL WRITE	Call subroutine WRITE

(ii) **Read:** Read register (N) on the selected chip (Y) to register 0 of the processor.

	Instruction	Comments
	LB 2, 15	
	LM N	
	LB 0, 15	
CLEAR	OTA	Register 0 should be cleared
	EXC–	
	GO CLEAR	
	LBL 0, Y	Y is the selected MM57126 chip number
	CALL READ	Call subroutine READ

SUBROUTINE

	Instruction	Comments
WRITE	RSC	Reset C register of processor to 0 for WRITE
	GO NEXT	
READ	SC	Set C register to 1 for READ
NEXT	OTA	
	ADX 5	READ/$\overline{\text{WRITE}}$ code to MM57126 will be a 0 if 5 is placed in A, and a 1 if A is 7
	NOP	
	TC	
	ADX 2	A = 7 in case of READ
	NOP	
	HXA	A ↔ H
	OTA	
	AX0	Clear the serial input/output port

	Instruction	S0	Comments
	BTD	0	Select MM57126 chip
	NOP	0	
NREADY	OTA	0	Check ready signal transition from high-to-low level (MM57126 is ready to communicate)
	AXO	0	
	ADX 1	0	
	GO READYH	0	
	OTA	0	
	AXO	0	
	NOP	0	
	GO NREADY	0	
READYH	OTA	0	
	AXO	0	
	ADX 1	0	
	GO READYH	0	
	HXA	0	Transfer READ or WRITE instruction pattern to I/O port to be shifted serially to MM57126
	AX0	0	
	NOP	1	
	OTA	R/W	
	LB 2, 15	1	Shift the register address (N) serially to MM57126, and point to M (0, 15)
	AX0	0	
	MTA 2	0	
	AX0	0	
CHECK	TC	RA_1	If it is the read instruction, go to the delay loop to allow I/O port be filled with first digit
	GO DELAY	RA_2	
REP	MTA	RA_3	
	AX0	RA_4	Shift 64 bits of data
	EXC–		
	GO REP		
	BTD		
	RET		
DELAY	NOP		Delay loop
	RSC		
	GO CHECK		

functional description (Continued)

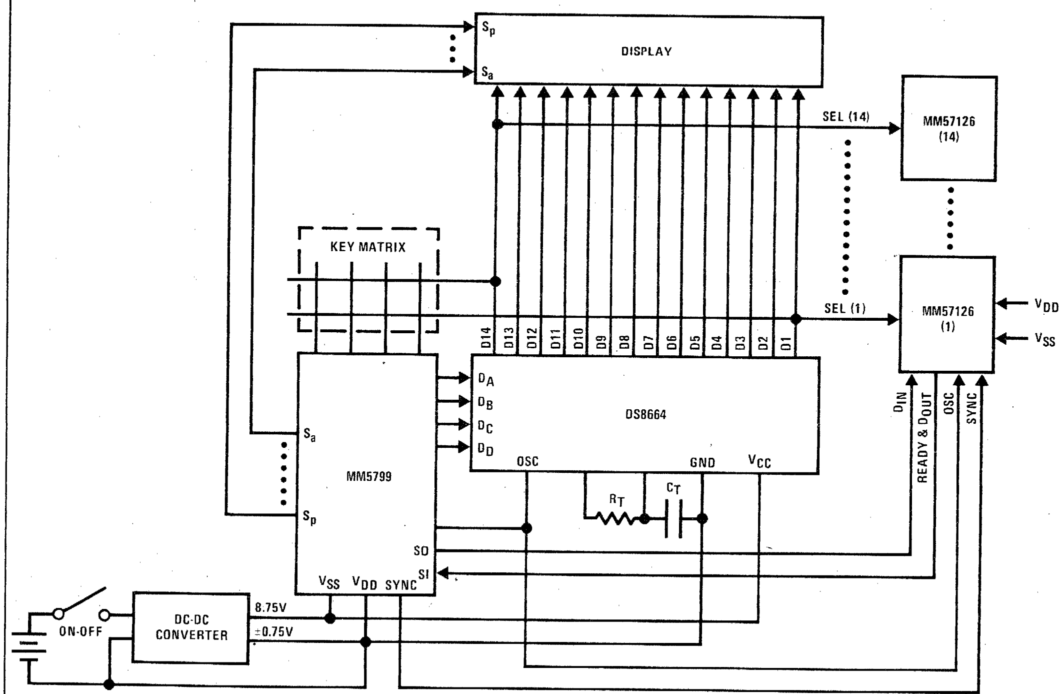


FIGURE 2. System Diagram

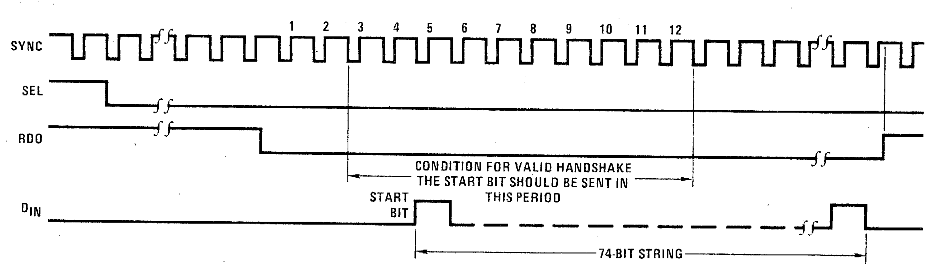


FIGURE 3. Timing Diagram for Handshaking Sequence

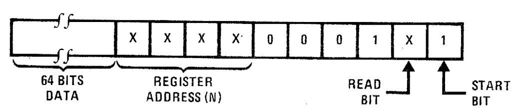


FIGURE 3a

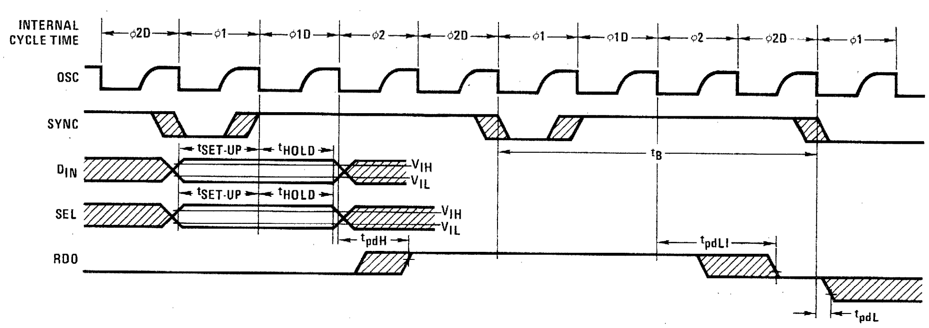
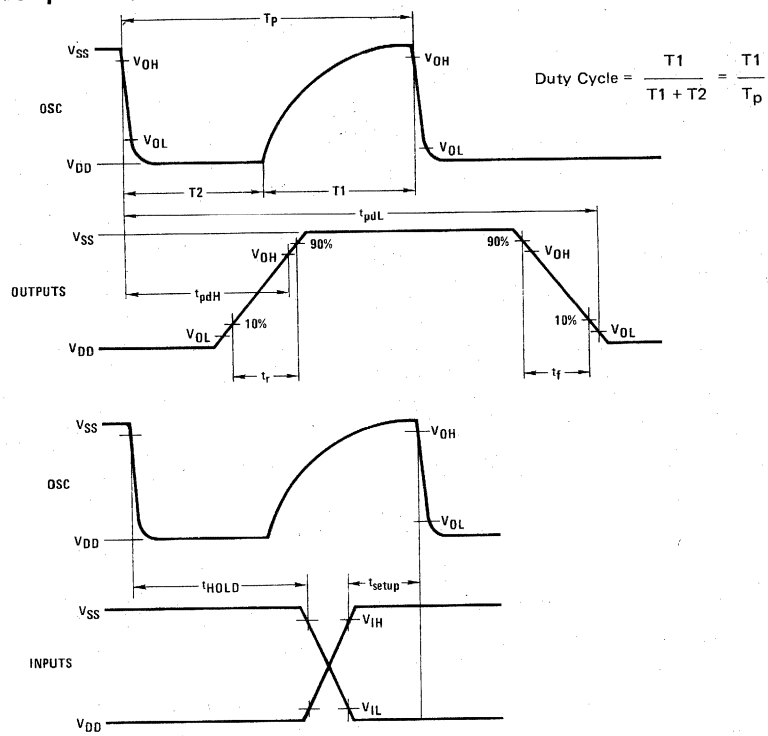


FIGURE 4

functional description (Continued)



Note. t_{SET-UP} is defined as time from osc. makes V_{OH} or V_{OL} transition to input V_{IH} or V_{IL} transition (ref. *Figure 4*, corresponding osc. time).

t_{HOLD} is defined as time from osc. makes V_{OH} or V_{OL} transition to input V_{IH} or V_{IL} transition (ref. *Figure 4*, corresponding osc. time).

FIGURE 5

MM57140 Controller Oriented Processor (COP)

general description

The MM57140 is an MOS/LSI device containing all system timing, arithmetic and logic, RAM, and control ROM functions required for implementation of a Controller Oriented Processor. It is capable of scanning up to 36 keyboard switches, or data may be entered as BCD data words through four input lines (K1–K4). Two general purpose inputs are available, and a third general purpose input shares an I/O pad with segment G. Nine output digits can be programmed as 1 of 9 (D1–D9), or as binary output on D1–D4, with a separate decoding of 1 of 5 on D5–D9. The segment outputs are mask programmable for either 7-segment output, or 4-bit binary output. All outputs on the MM57140 are latched, permitting the ROM to perform other functions while holding output data constant. Many options, and flexibility in programming permit the MM57140 to perform a large variety of customer-specified computations and control functions.

features

- 25 µs micro-instruction cycle time (typ)
- 630 micro-instruction ROM (8-bit instruction set)
- 220-bit RAM (55 digits)
- Four data or control inputs can provide keyboard scanning, or 4-bit binary inputs
- Three inputs directly accessible by the ROM (IN1, IN2, S_g/IN3) are available
- Internal power-on clear with mask programmable external override (IN1)
- ROM programmable latched digit outputs 1 of 9 multiplexing (D1–D9), or Binary (D1–D4), and 1 of 5 multiplexing (D5–D9)
- Mask programmable latched segment outputs, 7-segment or 4-bit binary
- Decimal point latched segment output
- General purpose latch output independent of segments
- Internal, or external oscillator
- Single power supply operation
- Direct segment drive of LED's
- Direct digit drive of LED's and TTL

block and connection diagrams

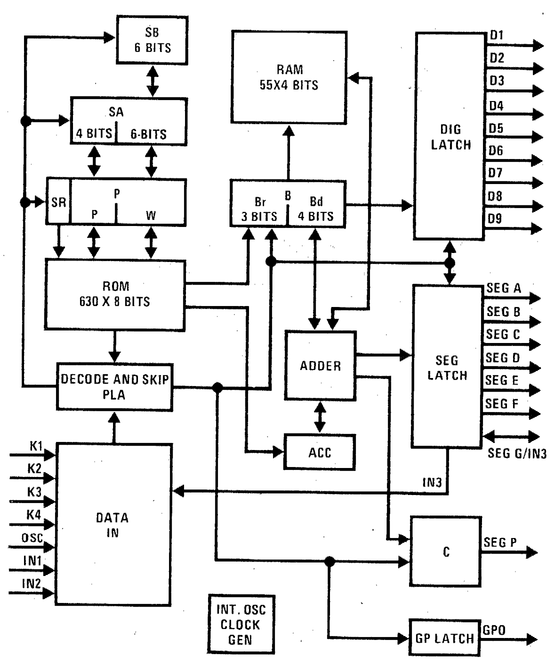
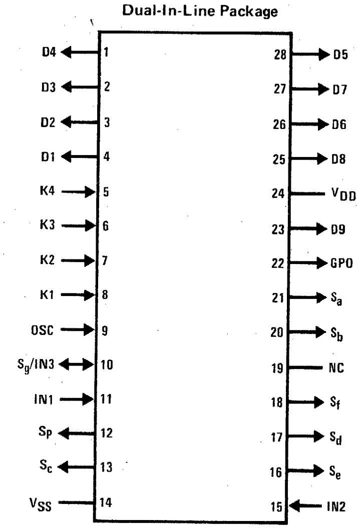


FIGURE 1. MM57140 Block Diagram

Dual-In-Line Package



TOP VIEW

Order Number MM57140N
See Package 23

Pin Descriptions

K1–K4	Keyboard Inputs
IN1, IN2, IN3	General Purpose Inputs
OSC	Programmable as External Oscillator
D1–D9	Digit Outputs
S_a–S_g	Segment Outputs
Sp	Decimal Point Segment Output
GPO	General Purpose Output
V_{DD}	–9 Volts
V_{SS}	0 Volts

MM57140

absolute maximum ratings

Volume at Any Pin Relative to V_{SS} (All Other Pins Connected to V_{SS})	V_{SS} +0.3V to V_{SS} −12V
Ambient Operating Time	0°C to +70°C
Ambient Storage Time	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$6.5V \leq V_{SS} - V_{DD} \leq 9.5V$

dc electrical characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Operating Supply Current	$V_{DD} = V_{SS} - 9.5V$, $T_A = 25°C$		8	15	mA
	Keyboard Scan Input Levels (K1–K4)					
V_{IH}	Logical High Level	$V_{DD} = V_{SS} - 6.5V$	V_{SS}−4.0		V_{SS}	V
		$V_{DD} = V_{SS} - 9.5V$	V_{SS}−4.0		V_{SS}	V
V_{IL}	Logical Low Level	$V_{DD} = V_{SS} - 6.5V$, $I_{IL} \leq \|-80\ \mu A\|$	V_{DD}		V_{SS}−6.0	V
		$V_{DD} = V_{SS} - 9.5V$, $I_{IL} \leq \|-80\ \mu A\|$	V_{DD}		V_{SS}−6.3	V
	Segment Output Current for Code = 40, 90	$V_{OUT} = V_{SS} - 1.0V$, $V_{DD} = V_{SS} - 6.5V$	|−2.5|			mA
		$V_{OUT} = V_{SS} - 5.0V$, $V_{DD} = V_{SS} - 8.0V$		−8		mA
		$V_{OUT} = V_{SS} - 6.5V$, $V_{DD} = V_{SS} - 9.5V$			|−12|	mA
	Segment Output Current for all Other Cases	See Performance Characteristics				
	IN1, IN2, IN3 Input Current	See Performance Characteristics				
	Digit Output Current					
I_{OH}	Logical High Level	$V_{OUT} = V_{SS} - 2.0V$, $V_{DD} = V_{SS} - 6.5V$	−300			μA
I_{OL}	Logical Low Level	$V_{OUT} = V_{SS} - 3.0V$	20			mA
	GPO Output	$V_{DD} = V_{SS} - 6.5V$				
V_{OH}	Logical High Level	$I_{OUT} = -550\ \mu A$	V_{SS}−1.0			V
V_{OL}	Logical Low Level	$I_{OUT} = 5\ \mu A$			V_{DD}+0.6	V
R_{KB}	Keyboard Resistance (K1–K4)				5	kΩ

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Ext. Osc. Frequency		70	160	280	kHz
Ext. Osc. Duty Cycle	*(Figure 2)*	40	50	60	%
Ext. Osc. Rise Time (T_r)				1	μs
Ext. Osc. Fall Time (T_f)	*(Figure 2)*			150	ns
GPO Transition Times	$V_{DD} = V_{SS} - 6.5V$, $C_L = 50$ pF				
High-to-Low				20	μs
Low-to-High				1	μs
Digit Output Transition Times	$V_{DD} = V_{SS} - 8.0V$, $C_L = 100$ pF				
High-to-Low			8		μs
Low-to-High			3		μs
Segment Output Transition Times	$V_{DD} = V_{SS} - 8.0V$, $C_L = 50$ pF				
High-to-Low					
Elec. Option Code = 10, 60			7.7		μs
11, 61			4.2		μs
20, 70			7.9		μs
21, 71			4.4		μs
22, 72			2.2		μs
30, 80			8.7		μs
31, 81			4.8		μs
32, 82			2.4		μs
Low-to-High					
Elec. Option Code = 10, 60			2.0		μs
11, 61			2.1		μs
20, 70			2.9		μs
21, 71			3.1		μs
22, 72			3.4		μs
30, 80			5.6		μs
31, 81			5.9		μs
32, 82			6.3		μs
Keyboard Inputs Low-to-High Transition Time After Key Release	$C_L = 25$ pF		6		μs

9

functional description

A block diagram of the MM57140 is shown in *Figure 1.* The control ROM is organized as 630 8-bit instruction words. ROM addressing is by a 10-bit Program Counter included in register P, a subroutine flag (SR), a 10-bit save register (SA), and a 6-bit save register (SB). This structure permits a one micro-cycle subroutine instruction to call a subroutine which is restricted to one specific page by setting SR, and a general two micro-cycle subroutine to call a subroutine on any page. Two levels of subroutine can be achieved by calling a restricted subroutine from a general subroutine.

The RAM contains 220 bits, addressed as 55 4-bit words. Data is formatted as 5 registers containing 11 digits each. (See *Figure 7.*)

Segment outputs are decoded by the segment PLA and brought out as either 7 segments, or 4-bit binary. The decimal position is brought out on the SEG P line. The segment, decimal point, and digit output buffers are capable of driving LED displays directly. Digit timing information for driving displays and external keyboard scanning is encoded into a 4-bit code (D1–D4) with 1 of 5 digits (D5–D9), or as 1 of 9 digits (D1–D9).

Four K inputs may be used for direct data inputs, or as key inputs scanned by internally decoded digit output lines (D1–D9) for up to 36 key keyboards. There are two additional inputs (IN1, IN2) which are available to the ROM. A third input (IN3) sharing a common I/O pad with Segment G is also available to the ROM.

The MM57140 has an internal power-on clear which is initiated when the V_{DD} supply has reached a nominal value of V_{SS} –6V. The power-on clear is then extended for an additional 1.0 ms. An external power-on clear can be provided with a mask option, through the use of IN 1, which overrides the internal clear when power supply turn-on time exceeds the 1.0 ms specification of the MM57140.

The digit outputs utilize non-refreshing bootstrap to achieve the high current sink capability (see dc electrical characteristics). Therefore, a software refresh must be used to toggle the digit outputs at least every 10 ms at room temperature and 1 ms at 50°C to continuously sink 20 mA. Otherwise, the depletion type load device will provide 10 µA sink current capability at V_{DD} + 1.0V without toggling digit outputs.

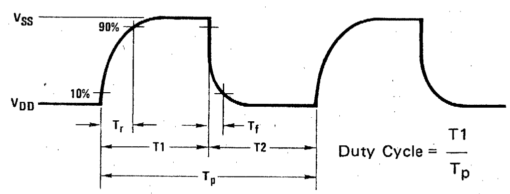


FIGURE 2. External Oscillator

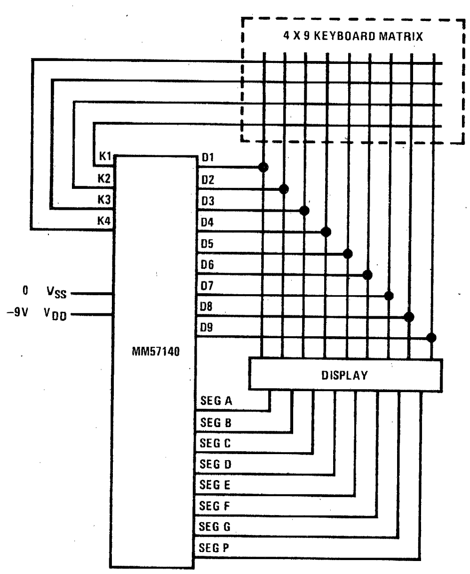


FIGURE 3. Low-Cost 9-Digit Calculator Using MM57140

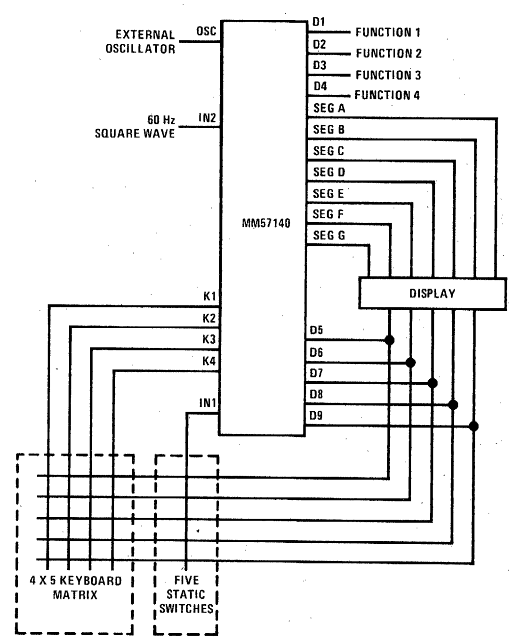


FIGURE 4. Clock and 4-Function Timer

functional description (Continued)

APPLICATIONS

The ROM, RAM, architecture of the MM57140 enables it to be used in a wide variety of control applications. Flexibility is achieved on the input and output line through the use of various mask options. *Figure 5 and Figure 6* illustrate the digit and segment options on the MM57140.

A low-cost calculator scheme, *(Figure 3)*, takes advantage of a 1 of 9 decode of the digit lines to scan a keyboard and provide timing signals for a 9-digit display. The segments are decoded as 7-segment outputs. Both segment and digit outputs drive calculator type LED displays directly.

Figure 4 suggests a circuit which permits the MM57140 to function as a clock with four presettable and resettable function outputs by using an alternate digit option. This clock provides time keyboard setting of digit on and off times for each of the four functions. Other applications requiring input, output as described in *Figures 5 and 6* may be provided by the MM57140 when ROM and RAM capacity coincide.

See Mask Programmable Options for the details of the options.

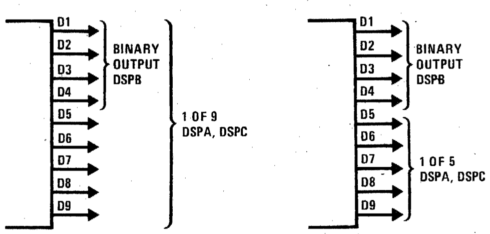


FIGURE 5. Digit Options

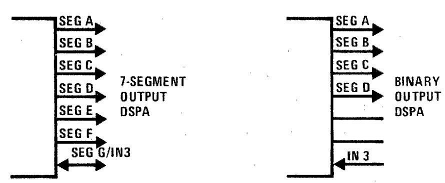


FIGURE 6. Segment Options

B4321 \ B765		r0 000	r1 001	r2 010	r3 011	r4 1XX	
d15	1111	0, 15	1, 15	2, 15	3, 15		
d14	1110	0, 14	1, 14	2, 14	3, 14		
d13	1101	0, 13	1, 13	2, 13	3, 13		D9
d12	1100	0, 12	1, 12	2, 12	3, 12		D8
d11	1011						D7
d10	1010						D6
d9	1001						D5
d8	1000						D4
d7	0111	0, 7	1, 7	2, 7	3, 7		D3
d6	0110	0, 6	1, 6	2, 6	3, 6		D2
d5	0101	0, 5	1, 5	2, 5	3, 5		D1

FIGURE 7. RAM Map

The indicated RAM cells are those that can be directly addressed by a single ROM instruction [LB(r, d)]. The output decoded lines are shown on the right-hand side vs the B(d) value before as DSPC command.

mask programmable options

1) Oscillator Options

DESCRIPTIONS	CODE
Internal Osc.	0
External Osc.	1

2) IN1 Options

DESCRIPTIONS		CODE	CURRENTS (NOTE 4)
Ext. Power "ON" (Pull-Up to V_{SS}) (Notes 1 and 2)		00	Source
Testable Input	Floating Input (Note 2)	10	
	Pull-Up to V_{SS} (Note 2)	11	Source
	Pull-Down to V_{DD} (Note 2)	12	Sink

mask programmable options (Continued)

3) IN2 Options

DESCRIPTIONS	CODE	CURRENTS (NOTE 4)
Floating Input (Note 2)	0	
Pull-Up to V_{SS} (Note 2)	1	Source
Pull-Down to V_{DD} (Note 2)	2	Sink

4) IN3 Options

(a) 7-Segment Outputs

DESCRIPTIONS	*CONDITIONS	CODE	CURRENTS (NOTE 4)
Floating Input (Note 3)	If Seg. Output Elec. Option is 00, 40, 50 or 90	00	
Pull-Up to V_{SS} (Note 3)	Seg. Output Elec. Option must be 00, 40, 50 or 90	01	Source
Pull-Down to V_{DD} (Note 3)	If Seg. Output Elec. Option is X0, X1 or X2, where X = 1, 2, 3, 6, 7, 8	02	Sink

*See segment output elec. options

(b) Segment as Binary Outputs

DESCRIPTIONS	CODE	CURRENTS (NOTE 4)
Floating Input (Note 2)	10	
Pull-Up to V_{SS} (Note 2)	11	Source
Pull-Down to V_{DD} (Note 2)	12	Sink

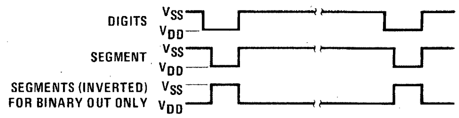
5) Digit Output Options

DESCRIPTIONS	CODE
*D1–D9 Multiplexed (1 of 9) by DSPC Only	00
*D1–D9 Multiplexed (1 of 9) by DSPA or DSPC	01
D1–D4 Binary Output by DSPB Only, D5–D9 Multiplexed (1 of 5) by DSPC Only	10
D1–D4 Binary Output by DSPB Only, D5–D9 Multiplexed (1 of 5) by DSPA or DSPC	11

*D1–D4 may be turned "ON" by DSPB

6) Segment Output Func. Options

DESCRIPTIONS	CODE
7-Segment Outputs	0
Binary Output (S_A–S_D)	1
Binary Output (S_A–S_D) Inverted	2



7) Segment Output Elec. Options

*DESCRIPTIONS (NOTE 4)		CODE	
DRIVER SIZE (MIL)	LOAD SIZE (MIL)	7-SEGMENT OUTPUTS	BINARY OUTPUTS
45/0.3		00	50
10/0.3	0.3/0.4	10	60
	0.55/0.4	11	61
20/0.3	0.3/0.4	20	70
	0.55/0.4	21	71
	1.1/0.4	22	72
45/0.3	0.3/0.4	30	80
	0.55/0.4	31	81
	1.1/0.4	32	82
45/0.3		40 (Note 5)	90 (Note 5)

*Segment source and sink currents are dependent upon the size of driver and load devices, respectively. Code 00, 40, 50 and 90 don't have current sinking capability.

8) Decimal Point Output Elec. Options

Same as 7-segment output elec. options.

9) Skip PLA Options

DESCRIPTIONS	CODE
EXC– Skips When B_d = 0, 4, 8, 12	3
EXC– Skips When B_d = 0, 8	7
EXC– Skips When B_d = 0, 4	11
EXC– Skips When B_d = 0, 1, 2, 3	12
EXC– Skips When B_d = 13, 15	16

Note 1: Internal power "ON" is still active but it will be overridden by external power "ON."

Note 2: State of the pin when the input is open.

Note 3: State of the pin when segment g output is turned "OFF."

Note 4: See Performance Characteristics for detail.

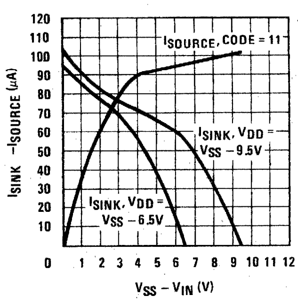
Note 5: Seg. output elec. option code 40, 90 are recommended for direct LED display. See dc electrical characteristics for current capability.

These nine options must be specified to program proper functions, inputs and outputs of the chip. Example. For on-chip osc. direct display calculator, the following options should be chosen:

1) Osc option – 0
2) IN1 option – 00
3) IN2 option – 2 (not used for calculator)
4) IN3 option – 00 (not used for calculator)
5) Digit output option – 01
6) Segment output func. option – 0
7) Segment output elec. option – 40
8) Decimal point output elec. option – 40
9) Skip PLA option – 12

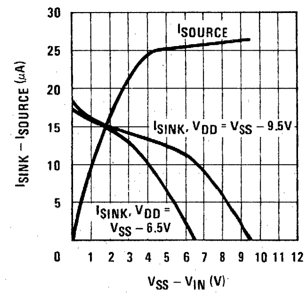
typical performance characteristics

IN1 Input Currents (Max)



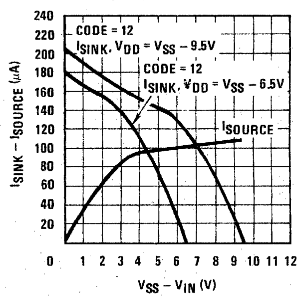
For IN1 code = 00, see IN2 characteristics.

IN2 Input Currents (Max)



1N1 (code = 00) source currents are same as IN2 source currents.

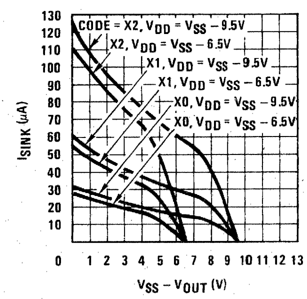
IN3 Input Currents (Max)



IN3 code = 02 is chosen and if segment output elec. option is

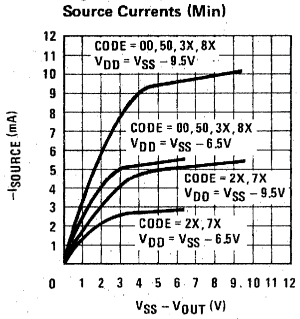
Code = X0, IN3 sink current is 1 times of code = 12
Code = X1, IN3 sink current is 1.84 times of code = 12
Code = X2, IN3 sink current is 3.67 times of code = 12
where X = 1, 2, 3, 6, 7, 8

Segment Output Sink Currents (Min)



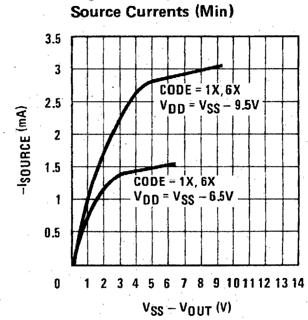
where X = 1, 2, 3, 6, 7, 8

Segment Output Source Currents (Min)



where X = 0, 1, 2

Segment Output Source Currents (Min)



where X = 0, 1, 2

standard instructions "0" = low = V_{DD}; "1" = high = V_{SS}

	MNEMONIC	DATA FLOW	STATUS – SKIP IF	DESCRIPTION
Arithmetic Operations	AD	$M + A \rightarrow A$		Add M(B) to A, Store sum in A.
	ADD	$C + M + A \rightarrow A$ $1 \rightarrow C$ Overflow	Overflow	Add carry bit to M(B). Add sum to A, store sum in A.
	SUB	$M + \bar{A} + C \rightarrow A$ Overflow → C	Overflow	Subtract A from M Overflow to C
	COMP	$\bar{A} \rightarrow A$		One's complement of A to A
	LAX (Y)	$Y \rightarrow A$		$Y \rightarrow A$ Y = 0 – 15
	ADX (Y)	$A + Y \rightarrow A$	No overflow	Add constant (Y) to A. Store sum in A. Y = 1, 2. . .15.
	TAM		A = M(B)	Compare contents of A to M(B), skip if A = M(B)
	SC	$1 \rightarrow C$		Set C register
	RSC	$0 \rightarrow C$		Reset C register
	TC		C = 0	Skip if C = 0
Input/Output	DSPA*	$A \rightarrow S_a - S_g$, $C \rightarrow S_p$		A to output latches, 7-segment decoded to $S_a - S_g$. Segment decode is programmable. (7-segment or 4-bit binary). C to S_p latch.
	DSPB	B4 – B1 → D4 – D1		B4 – B1 to digit output latches D4 – D1
	DSPC*	B4 – B1 → D9 – D1	Always Skips	B4 – B1 decoded to digit output latches, (1 of 9), $B_d = S \rightarrow 13$
	RGPO	Reset Output		GPO is latched to V_{SS}
	SGPO	Set Output		GPO is latched to V_{DD}
	READ	K4 – K1 → A		Read K inputs to A
Input Test	TIN1		IN1 = 1	Test IN1
	TIN2		IN2 = 0	Test IN2
	TKB		K = 0	Skip if any K input active.
	TIN3		IN3 = 0	Test IN3 (SEG g)
Control Functions	GO	$I_6 - I_1 \rightarrow P$		Load next ROM instruction address.
	CALL	If ($\overline{LG}$) SET – SR $I_6 - I_1 \rightarrow P$, $SA_W \rightarrow SB_W$, P+1 → SA		Call subroutine. If previous instruction was not LG, set SR.
	RET	$SA_W \rightarrow P_W$ If ($\overline{SR}$) $SA_P \rightarrow P_P$ $SA_W \leftrightarrow SB_W$		Pop up ROM address save registers. 0 SR
	LG/GO	$I_4 - I_1 \rightarrow P_p$ $I_6 - I_1$ (Second Word) → P_W		Two micro-cycle operation. Long GO TO, Load P_p and P_W.
	LG/CALL	SA → SB, P + 1 → SA $I_6 - I_1$ (Second Word) → P_W		Two micro-cycle operation. Long call. Load Pp and P_W. Push down address save registers.
	NOP			No operation.
Memory Digit Operations	EXC (r)	$A \leftrightarrow M(B)$ $B_r \oplus r \rightarrow B_r$		Exchange data word at M(B) with A EXCLUSIVE-OR B_r with r. r = 0, 1, 2, 3
	EXC –(r)	$A \leftrightarrow M(B)$ $B_r \oplus r \rightarrow B_r$, $B_d - 1 \rightarrow B_d$	$B_d \rightarrow 3, 2, 1, 0$	Exchange and decrement B EXCLUSIVE-OR B_r with r. r = 0, 1, 2, 3
	EXC +(r)	$A \leftrightarrow M(B)$ $B_r \oplus r \rightarrow B_r$, $B_d + 1 \rightarrow B_d$	$B_d \rightarrow 13$	Exchange and increment B_d EXCLUSIVE-OR B_r with r. r = 0, 1, 2, 3
	MTA (r)	$M(B) \rightarrow A$ $B_r \oplus r \rightarrow B_r$		Load accumulator with data word M(B) EXCLUSIVE-OR B_r with r. r = 0, 1, 2, 3
Memory Bit Operations	TM (Z)		M (B, Z) = 0	Test bit Z of M(B), skip if zero Z = 1, 2, 4, 8
Memory Address Operations	LB (r,d)	$r \rightarrow B_r$, $d \rightarrow B_d$		r = 0, 1, 2, 3. d = 5, 6, 7, or 12, 13, 14, 15
	ATB	$A \rightarrow B_d$		Transfer contents of accumulator to B_d register
	BTA	$B_d \rightarrow A$		Transfer contents of B_d register to accumulator
	SB7	Set B7		Sets B7. 5th register is addressed independent of B5 and B6.
	RB7	Reset B7		B5 and B6 are unchanged

*DSPA can be programmed to turn on DSPC.