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Section 3
F8 Microcomputer Family

General

The distribution of logic among the various elements of a microcomputer system is one of the most variable features of such systems. The traditional division of logic corresponds to the requirements of a computer; e.g., one device serving as CPU, one as memory, and one as I/O. In the F8 microcomputer family, logic is implemented in devices in terms of application complexity rather than in terms of computer function. Thus, for example, two F8 devices implement all of the basic functions of a small microcomputer.

To accomplish this, the design of the F8 family includes a number of non-traditional function assignment features:

1. A small amount of RAM is implemented within the CPU as a scratchpad memory.
2. Memory addressing logic is implemented in the memory devices rather than in the CPU.
3. The I/O ports are implemented in the CPU and memory devices rather than in discrete I/O devices.

Every F8 configuration must contain an F3850 CPU, at least one F3851 Program Storage Unit (PSU) or memory interface device, and standard ROM or PROM (see figure 3-1). The memory-oriented devices may be used singly or together in the same system; when necessary, multiple units of the same type may be used. For example, an F3850 and two F3851s may comprise a system requiring 2K words of ROM, 64 bytes of RAM, and six I/O ports.

Memory Interface Devices

When required by the application, the F3851 PSU may be replaced by an F3853 Static Memory Interface (SMI). Both of these devices interpret control signals output by the F3850 and generate the standard address and control signals required by off-the-shelf dynamic and static memory devices.

Input/Output Devices

Applications that require additional I/O and interrupt capabilities but do not require the PSU storage capacity can make use of the F3861 Peripheral Input/Output (PIO) device. The PIO, which also contains interrupt logic and a programmable timer, interprets CPU control signals to drive two 8-bit I/O ports.

Bus Structure

The F8 microcomputer components are interconnected by means of a system bus structure that is composed of the following elements:

1. Eight data bus lines (DB_0 – DB_7)
2. Five control lines ($ROMC_0$ – $ROMC_4$)
3. Two clock lines (Φ, WRITE)
4. Three interrupt lines (PRI IN, PRI OUT, INT REQ)

Instruction Set

The instruction set of a microprocessor or microcomputer is the software tool used to shape the device or system for a particular application. The F8 instruction set is divided into four functional groups.

1. Input/Output
2. Arithmetic/Logical
3. Address Register Control
4. Indirect Scratchpad Address Register (ISAR) and Status Control

The F8 instruction set is presented in table 3-1.

Table 3-1 F8 Instruction Set

Instruction	Description
ADC	Add Accumulator to Data Counter
AI	Add Immediate to Accumulator
AM	Add (Binary) Memory to Accumulator
AMD	Add (Decimal) Memory to Accumulator
AS	Add (Binary) Scratchpad Memory to Accumulator
ASD	Add (Decimal) Scratchpad Memory to Accumulator
BC	Branch on Carry
BF	Branch on false
BM	Branch on Negative
BNC	Branch if No Carry
BNO	Branch if No Overflow
BNZ	Branch if Not Zero
BP	Branch if Positive
BR	Unconditional Branch
BR7	Branch on ISAR
BT	Branch on True
BZ	Branch on Zero
CI	Compare Immediate
CLR	Clear Accumulator
COM	Complement
DCI	Load Data Counter Immediate
DI	Disable Interrupt
DS	Dessement Scratchpad Memory Content
EI	Enable Interrupt
IN	Input Long Address
INC	Increment Accumulator
INS	Input Short Address
JMP	Branch Immediate
LI	Load Immediate
LIS	Load Immediate Short
LISL	Load Lower Octal Digit of ISAR
LISU	Load Upper Octal Digit of ISAR
LM	Load Accumulator from Memory
LNK	Link Carry to Accumulator
LR	Load Register
NI	AND Immediate
NM	Logical AND from Memory
NOP	No Operation
NS	Logical AND from Scratchpad Memory
OI	OR Immediate
OM	Logical OR from Memory
OUT	Output Long Address
OUTS	Output Short Address
PI	Call to Subroutine Immediate
PK	Call to Subroutine Direct and Return from Subroutine Direct
POP	Return from Subroutine
SL	Shift Left
SR	Shift Right
ST	Store to Memory
XDC	Exchange Data Counters
XI	Ekxclusive-OR Immediate
XM	Exclusive-OR from Memory
XS	Exclusive-OR from Scratchpad Memory

Descriptions

Following is data that describes the members of the F8 microcomputer system family.

F8 FAMILY ORGANIZATION